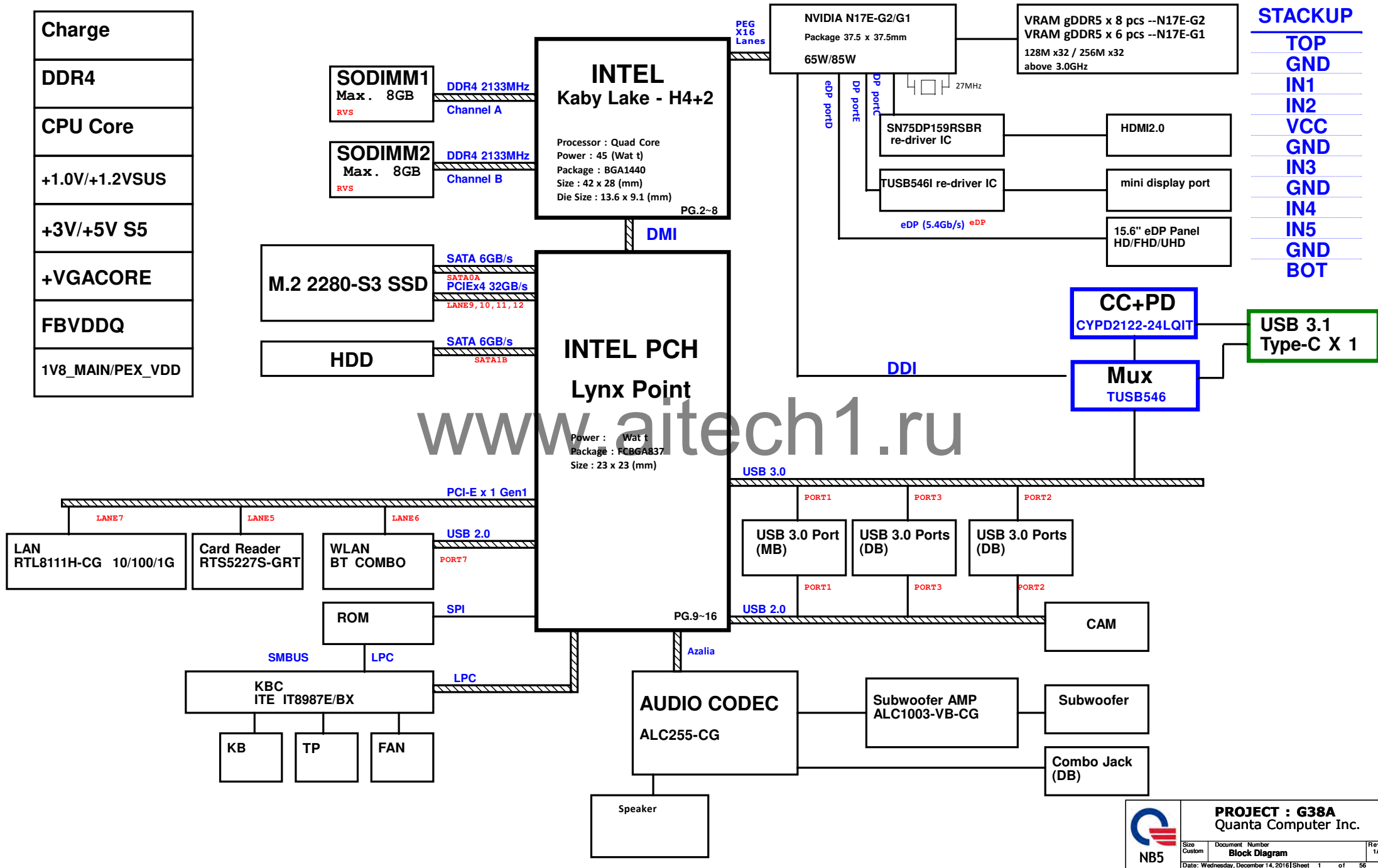


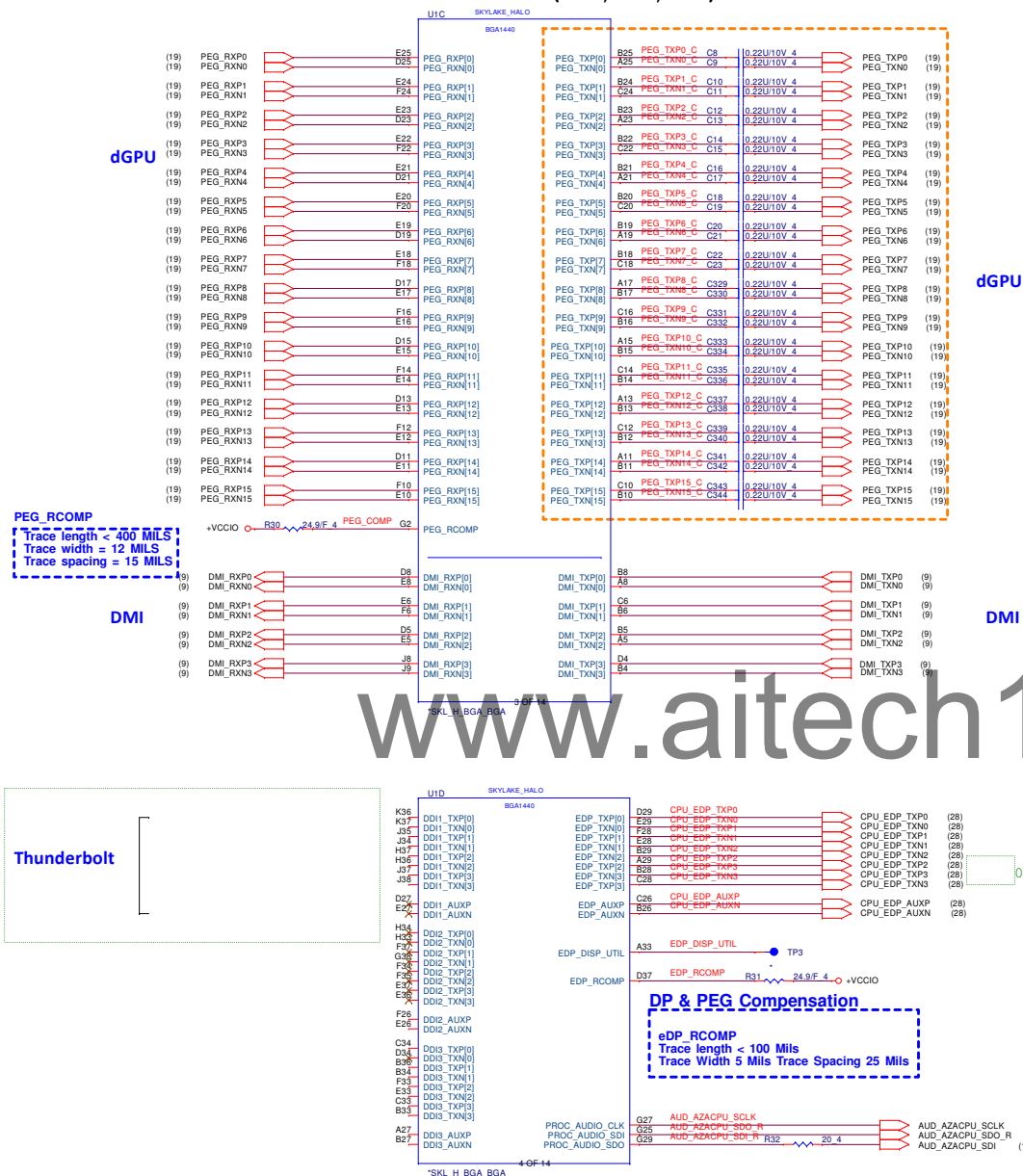
NL5/NL5A N17E-G1/G2 INTEL KABY -H SYSTEM DIAGRAM

01



Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

The diagram illustrates a 13-channel optical OFDM transmitter. It features a central vertical bus structure. On the left, a green box represents the control and monitoring section, connected to the first channel (CFG1). The main body of the transmitter consists of 13 parallel channels, each labeled CFG1 through CFG13. Each channel includes a laser source, a phase shifter, a modulator, and a filter. The channels are connected to a common output bus on the right. The diagram also shows the electrical and optical components of the transmitter, including the laser, modulator, and filter.

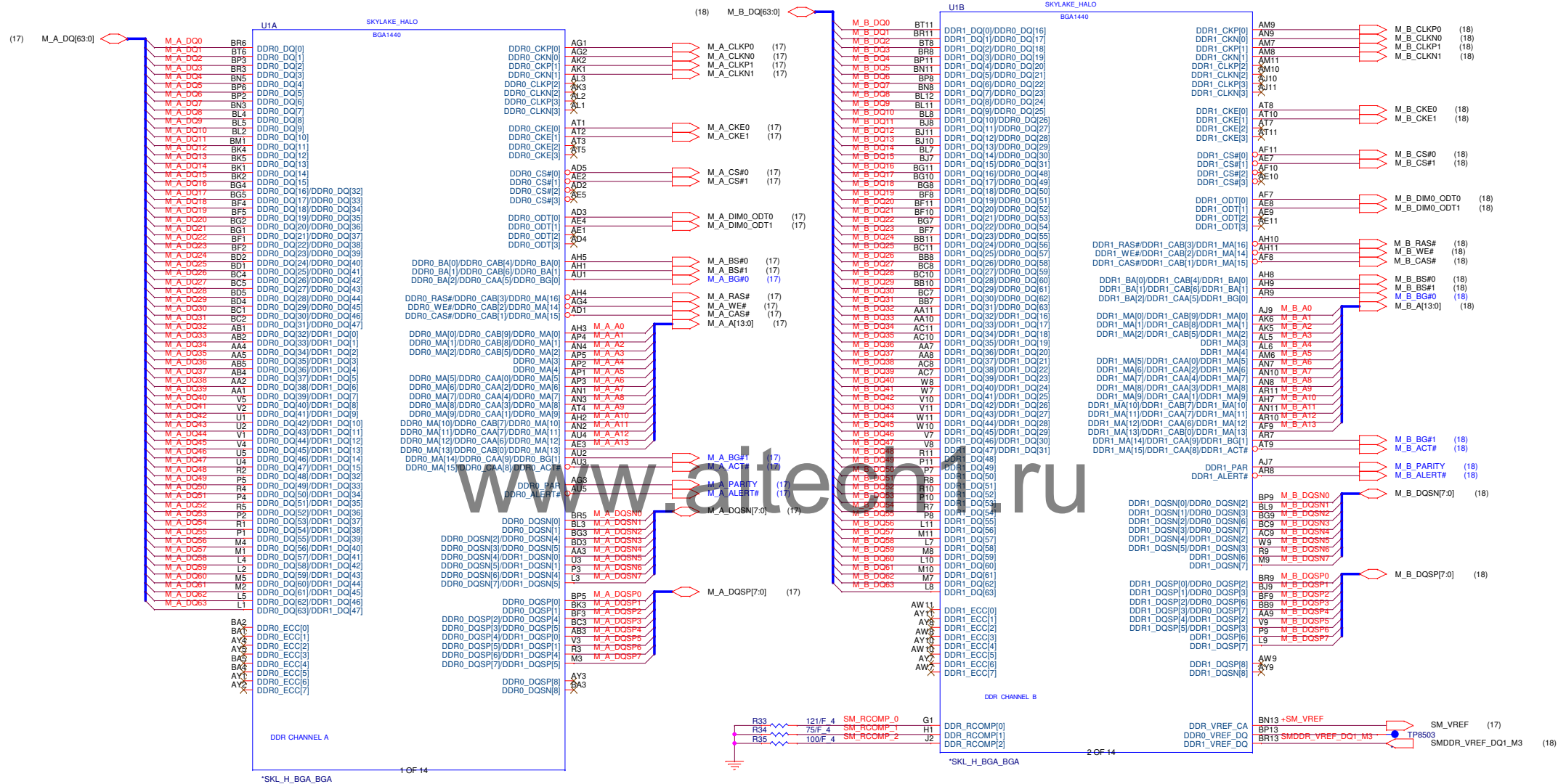


```
0801  Add
0805  DEL
0822  Modify
```

Thunderbolt


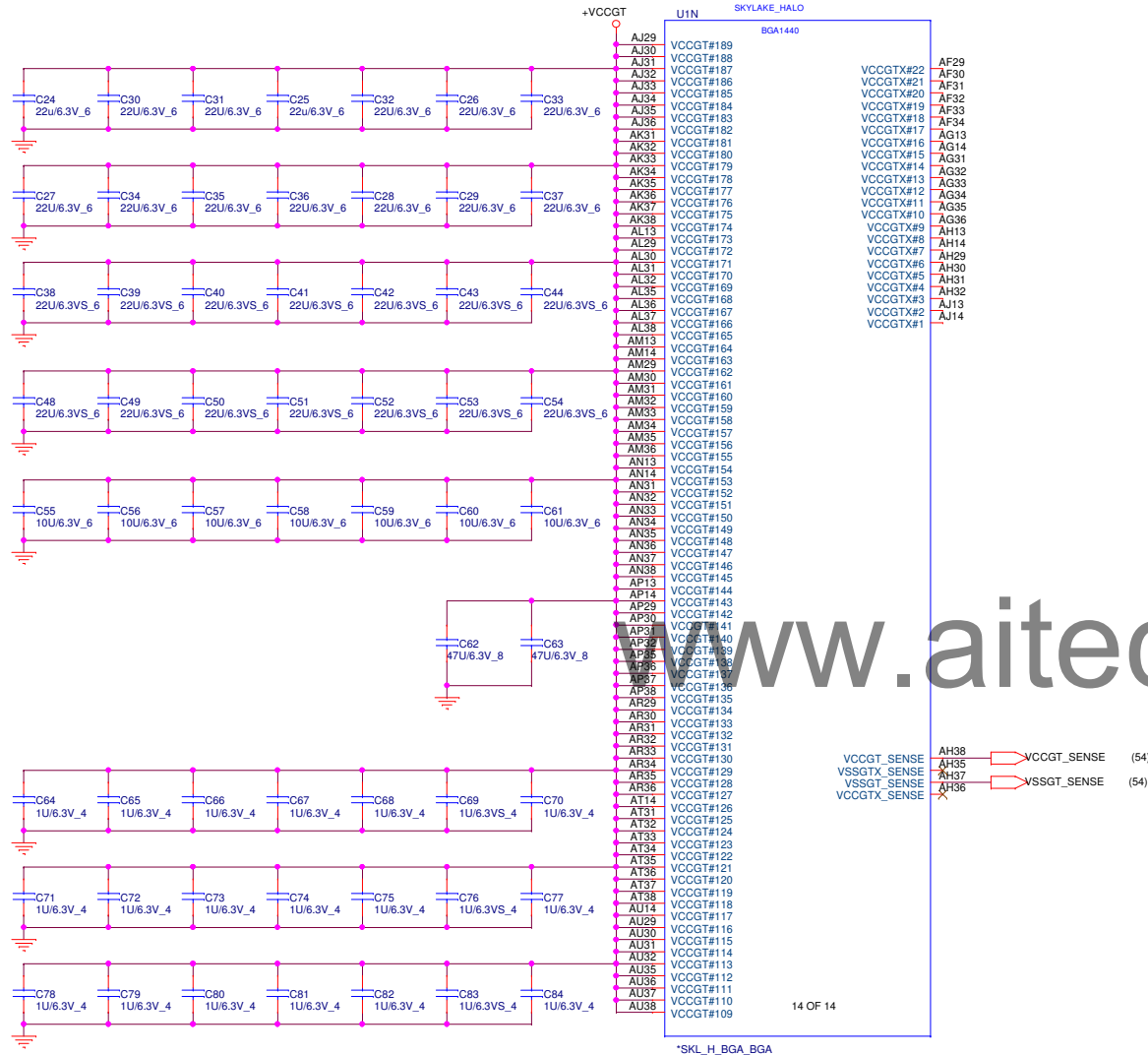
0819 Add

SKYLAKE Processor (DDR4)



SKYLAKE Processor (POWER)

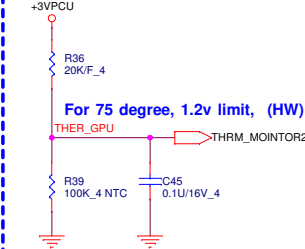
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

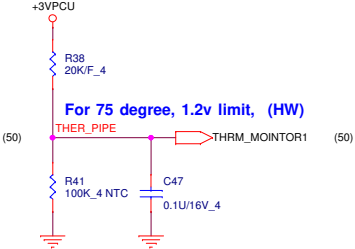
IO Thrm Protect

Location need thermal confirm

For GPU USE



For CPU USE



0801 Del CPU thermal IC

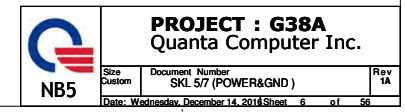
CPU Thermal Sensor

Location need thermal confirm

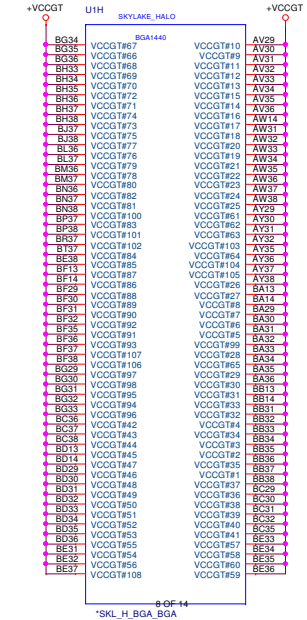
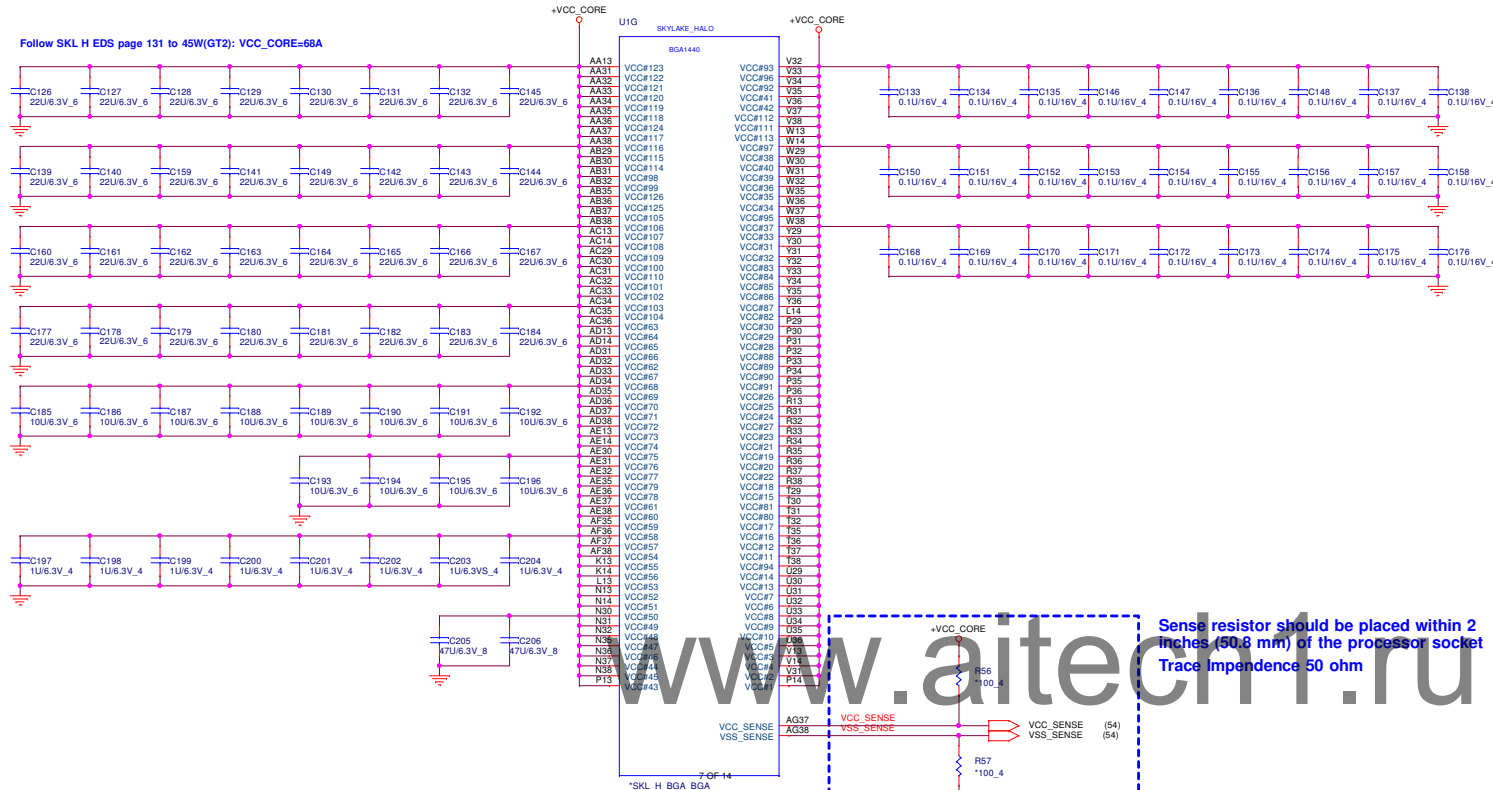
0801 Del GPU thermal IC

GPU Thermal Sensor

Follow SKL H EDS page 135 45W: VDDQ=2.8A



Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A



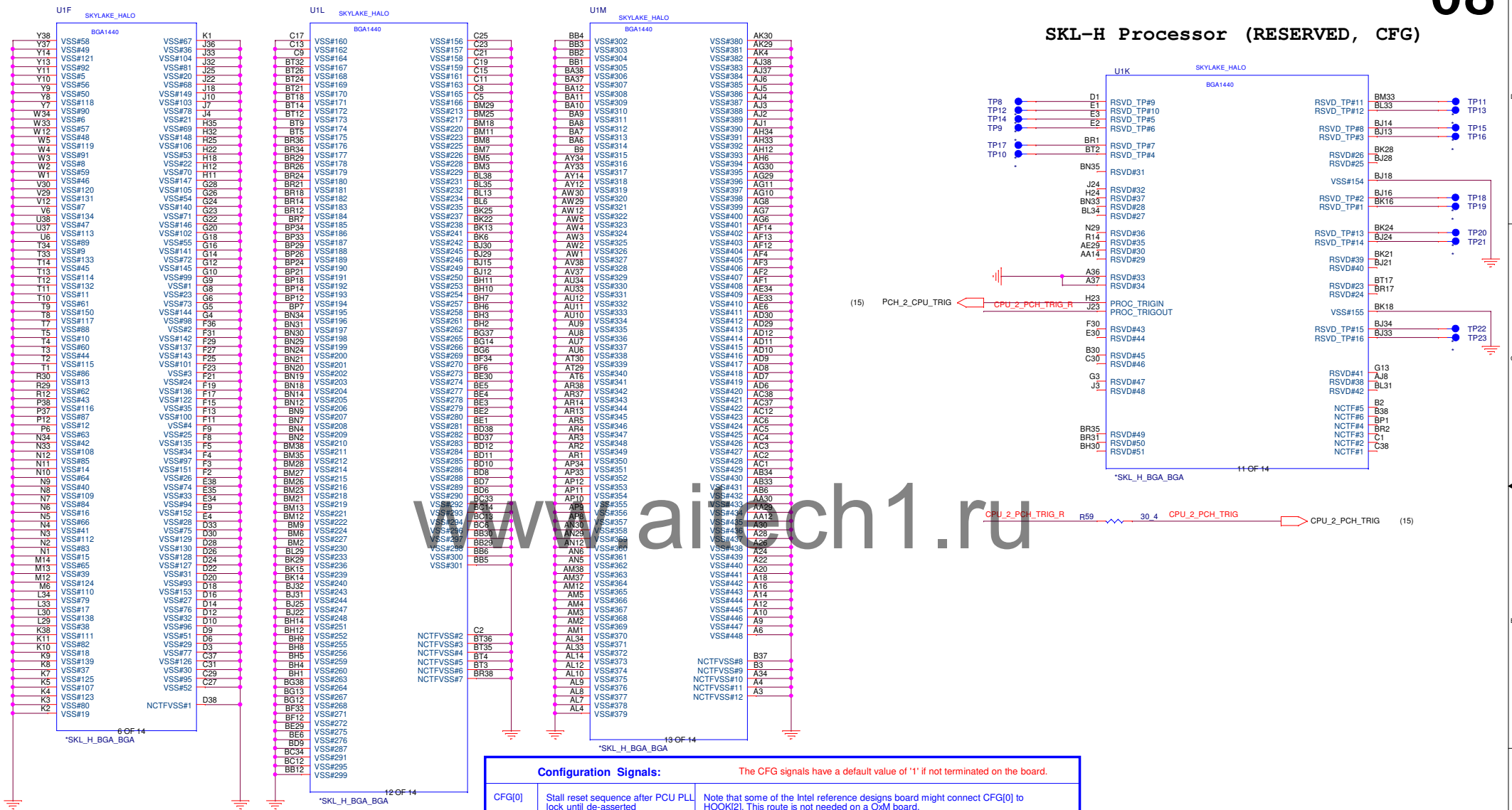
+VCC_CORE (54.55)



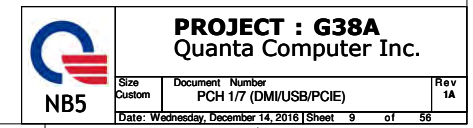
PROJECT : G38A
Quanta Computer Inc.

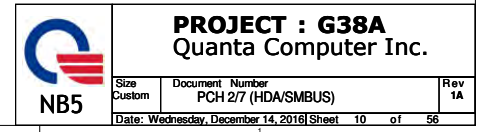
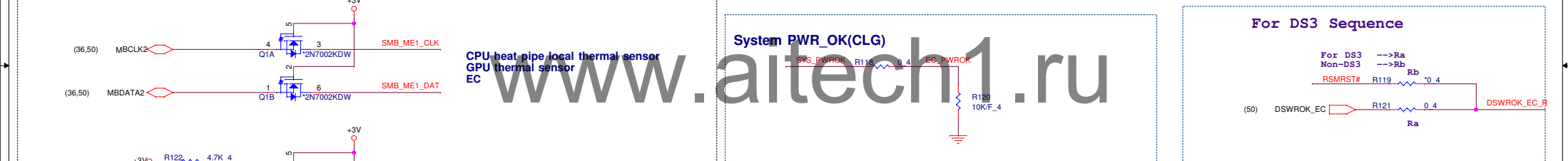
Size	Document Number	Rev
Custom	SKL 6/7 (POWER&GND)	1A
Date: Wednesday, December 14, 2014		Sheet 7 of 56

SKL-HPprocessor (GND)



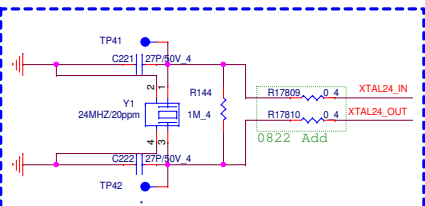
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	





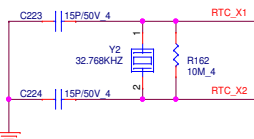
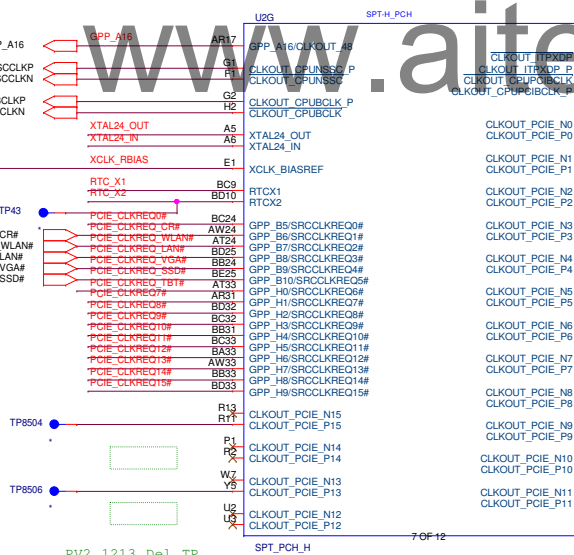


The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

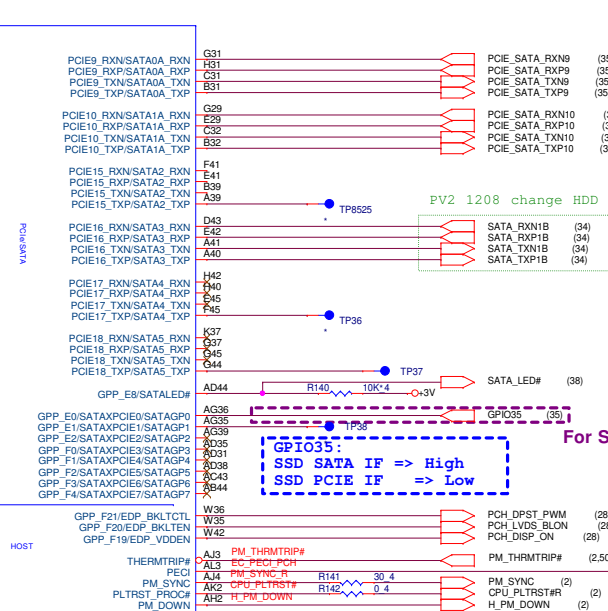


Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out: 4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz

[illegible]

PV2 1213 Del TP



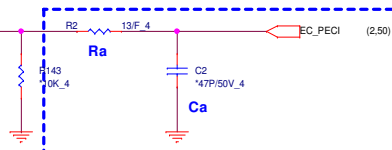
SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

PV2 1208 change HDD port

For SSD Det (SATA0A)

BOM:SSD only



H_PECI (50ohm)
Trace Length: <0.5 inches
Ba.Ca. need placement close to PCH.

Card Reader

(35) WLAN

1) LAN

VGA

15) **SSD**

There

BOM:DIS only

BOM:SSD only

0801 Add

PLTRST#(CLG)



Ra
Rb

Support HW TPM -->Ra
Support SW TPM -->Rb (default)

PCH SPI ROM(CLG)



Place to TOP



PCH Strap Pin

BOOT SELECT STRAP
HIGH: LPC
LOW: SPI. (Default)

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

ESPI FLASH SHARING MODE

HIGH: SLAVE ATTACHED FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW

DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL

TOP SWAP OVERRIDE STRAP
HIGH: TOP SWAP ENABLED (CRB)
LOW: TOP SWAP DISABLED (DEFAULT)

TLS CONFIDENTIALITY ENABLED
HIGH: Flash Descriptor Security (override). This
strl.tnY.GldmL.OF.OmY/xmY.yUx.im/mVl.mUmU.Ul.mYsOp.Csmplng.sV/FYxYxmY.hmlL.Umx.mVUUl.(mLpL.oF.OmY/xmY.xYmL.mYuh.OmY/xul duxGox
LOW: security measures defined in the Flash Descriptor. (Default)

RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

RING OSCILLATOR BYPASS

XTAL INPUT FREQUENCY[0]

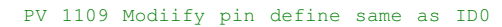
XTAL INPUT FREQUENCY[1]

TLS CONFIDENTIALITY ENABLED
HIGH: T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

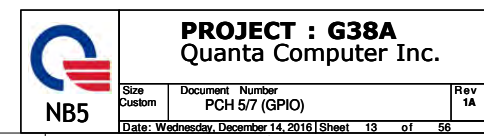
RESERVED
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

RESERVED

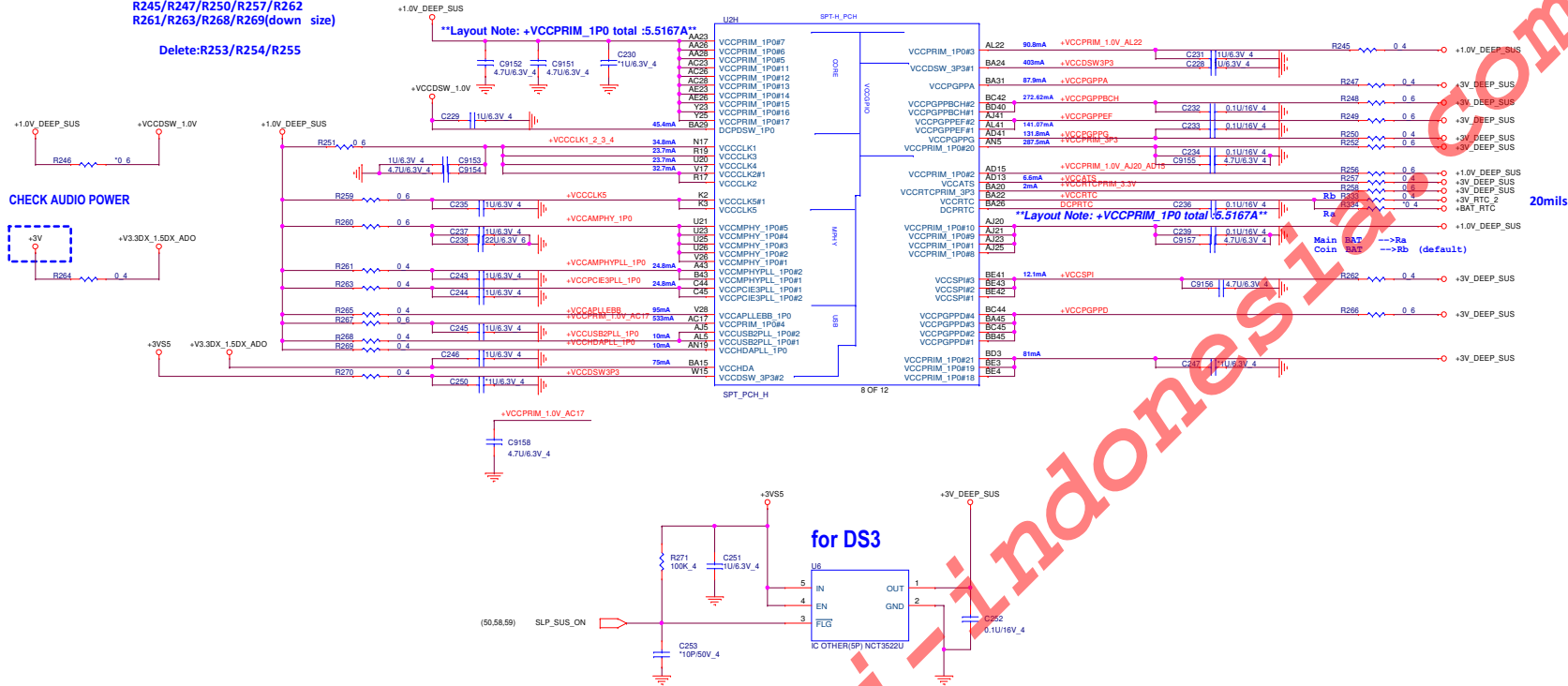
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



	GPU STRAP5
G-SYNC	100K PU (R12060)
None G-SYNC	100K PD (R12061)



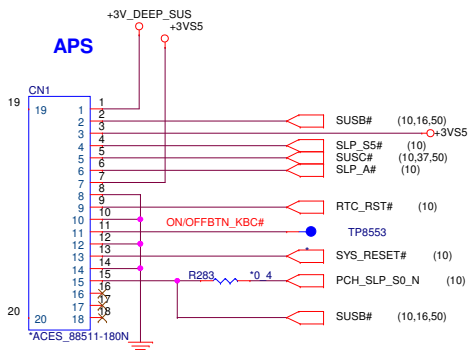
R245/R247/R250/R257/R262
R261/R263/R268/R269(down size)
Delete:R253/R254/R255




(9,10,12,13,16) +3V_DEEP_SUS 



www.teknisi-indonesia.com



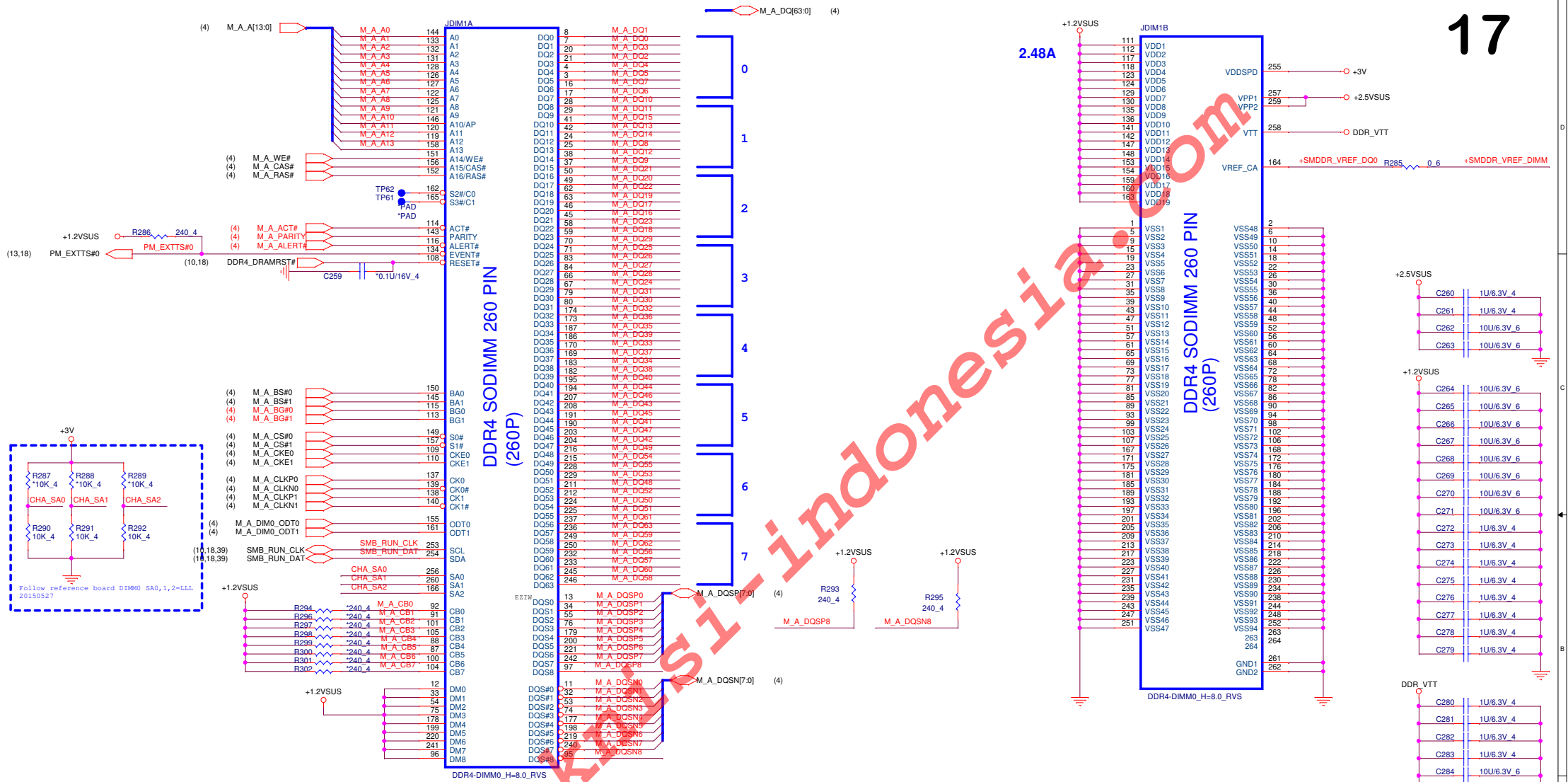
(9,10,12,13,14) +3V_DEEP_SUS



PROJECT : G38A
Quanta Computer Inc.

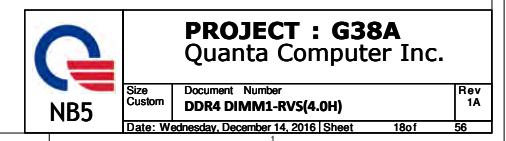
Size	Document Number	Rev
	NDP & APS	1A

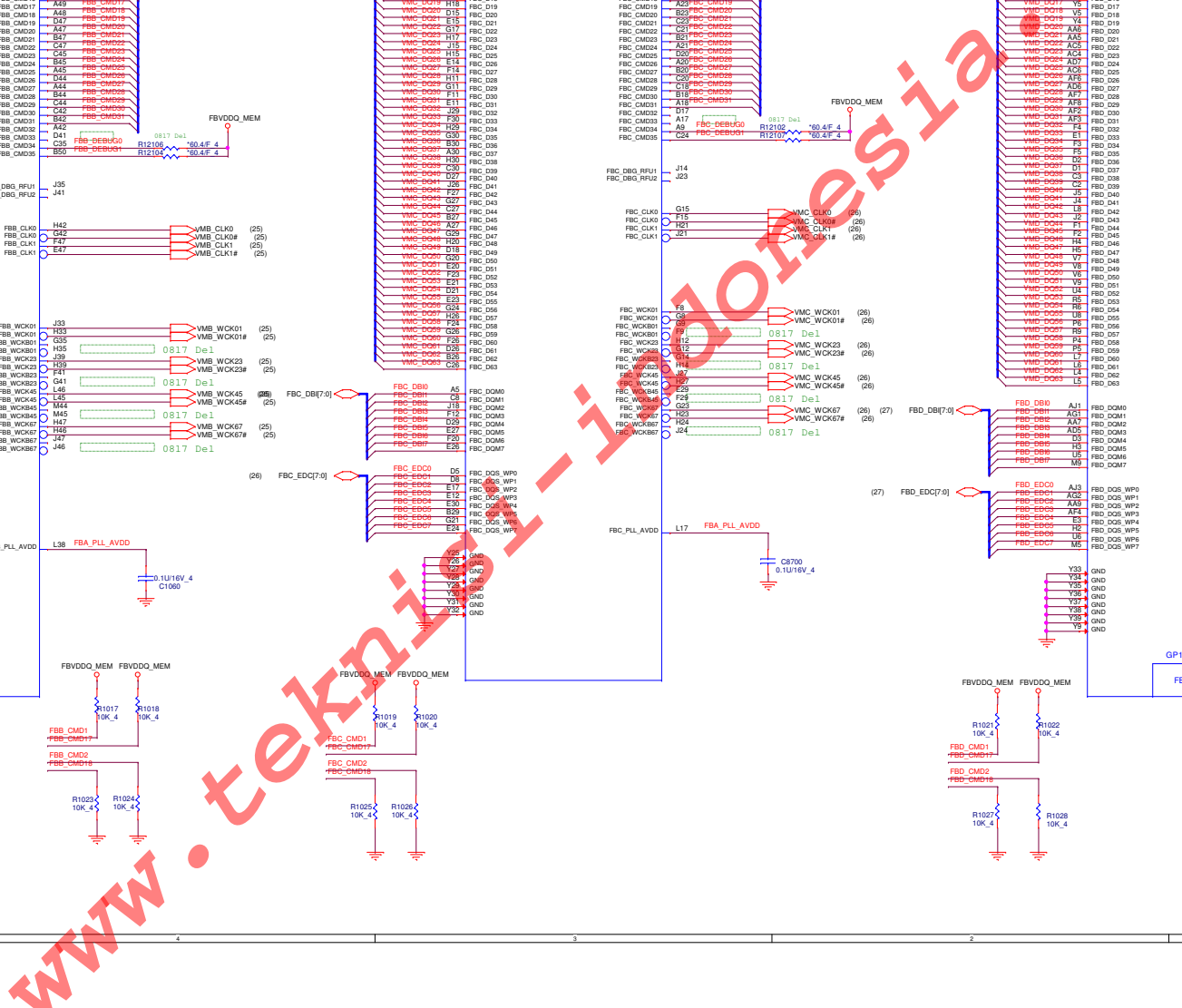
Date: Wednesday, December 14, 2016 | Sheet 16 of 56



+2.5VSUS (18,53)
 DDR_VTT (18,53)
 +1.2VSUS (2,6,10,18,53,59,64)
 +3V (9,10,11,12,13,14,18,21,22,28,30,31,32,33,35,38,39,41,42,44,50,54,57,63)

NB5	PROJECT : G38A Quanta Computer Inc.		
	Size Custom	Document Number DDR4 DIMM0-STD(4.0H)	Rev 1A
Date: Wednesday, December 14, 2016 Sheet 17 of 56			





Strap Pins <small>1000 Models</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory BvL for memory configs corresponding to these numbers)
L	L	L	0 (0x000)
L	L	H	1 (0x001)
L	H	L	2 (0x002)
L	H	H	3 (0x003)
H	L	L	4 (0x004)
H	L	H	5 (0x005)
H	H	L	6 (0x006)
H	H	H	7 (0x007)
M	L	M	8 (0x008)
L	M	L	9 (0x009)
M	M	M	10 (0x000A)

Table 1. HTF-G1-G2 (2005) Recommended Member

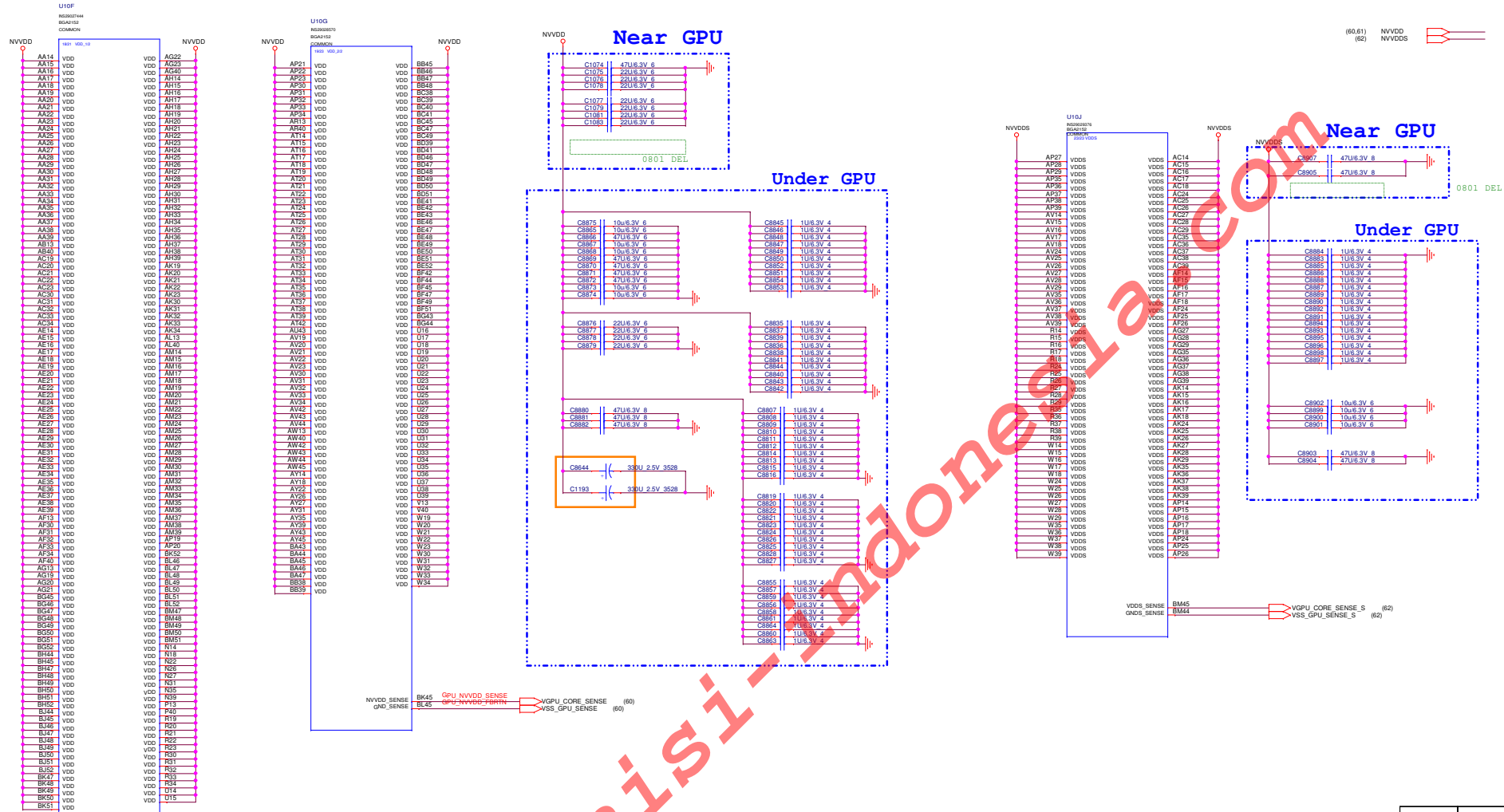
Member Grade	General Classification	Span (m)	Depth (m)	Designation	Max Span (m)	Max Depth (m)	Max Clearance (m)	Max Weight (kN)	Max Wind (kN)	Max Wind (kN)	Max Wind (kN)	Max Wind (kN)
1/2	TH4002	1.00	1.00	HTF-G1-G2-1/2-1.00-1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
		1.00	1.00	HTF-G1-G2-1/2-1.00-1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	
		1.00	1.00	HTF-G1-G2-1/2-1.00-1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	
		1.00	1.00	HTF-G1-G2-1/2-1.00-1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	

HTF-G1-G2 (2005) Recommended Member

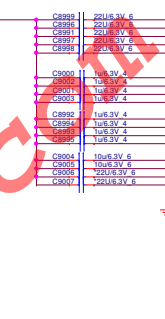
SPID	SPNAME	CS	Platform Description	CS Description
SP001	SP001_VPROC_PBA_VBI	1	Full System Image (FSI) for CS-1	CS1 Transmittance
SP002	CS001	1	Full System Image (FSI) for CS-1	CS1 Transmittance
SP003	CS002	1	Full System Image (FSI) for CS-2	CS2 Transmittance
SP004	CS003	1	Full System Image (FSI) for CS-3	CS3 Transmittance
SP005	CS004	1	Full System Image (FSI) for CS-4	CS4 Transmittance
SP006	CS005	1	Full System Image (FSI) for CS-5	CS5 Transmittance
SP007	CS006	1	Full System Image (FSI) for CS-6	CS6 Transmittance
SP008	CS007	1	Full System Image (FSI) for CS-7	CS7 Transmittance
SP009	CS008	1	Full System Image (FSI) for CS-8	CS8 Transmittance
SP010	CS009	1	Full System Image (FSI) for CS-9	CS9 Transmittance
SP011	CS010	1	Full System Image (FSI) for CS-10	CS10 Transmittance
SP012	CS011	1	Full System Image (FSI) for CS-11	CS11 Transmittance
SP013	CS012	1	Full System Image (FSI) for CS-12	CS12 Transmittance
SP014	CS013	1	Full System Image (FSI) for CS-13	CS13 Transmittance
SP015	CS014	1	Full System Image (FSI) for CS-14	CS14 Transmittance
SP016	CS015	1	Full System Image (FSI) for CS-15	CS15 Transmittance
SP017	CS016	1	Full System Image (FSI) for CS-16	CS16 Transmittance
SP018	CS017	1	Full System Image (FSI) for CS-17	CS17 Transmittance
SP019	CS018	1	Full System Image (FSI) for CS-18	CS18 Transmittance
SP020	CS019	1	Full System Image (FSI) for CS-19	CS19 Transmittance
SP021	CS020	1	Full System Image (FSI) for CS-20	CS20 Transmittance
SP022	CS021	1	Full System Image (FSI) for CS-21	CS21 Transmittance
SP023	CS022	1	Full System Image (FSI) for CS-22	CS22 Transmittance
SP024	CS023	1	Full System Image (FSI) for CS-23	CS23 Transmittance
SP025	CS024	1	Full System Image (FSI) for CS-24	CS24 Transmittance
SP026	CS025	1	Full System Image (FSI) for CS-25	CS25 Transmittance
SP027	CS026	1	Full System Image (FSI) for CS-26	CS26 Transmittance
SP028	CS027	1	Full System Image (FSI) for CS-27	CS27 Transmittance
SP029	CS028	1	Full System Image (FSI) for CS-28	CS28 Transmittance
SP030	CS029	1	Full System Image (FSI) for CS-29	CS29 Transmittance
SP031	CS030	1	Full System Image (FSI) for CS-30	CS30 Transmittance
SP032	CS031	1	Full System Image (FSI) for CS-31	CS31 Transmittance
SP033	CS032	1	Full System Image (FSI) for CS-32	CS32 Transmittance
SP034	CS033	1	Full System Image (FSI) for CS-33	CS33 Transmittance
SP035	CS034	1	Full System Image (FSI) for CS-34	CS34 Transmittance
SP036	CS035	1	Full System Image (FSI) for CS-35	CS35 Transmittance
SP037	CS036	1	Full System Image (FSI) for CS-36	CS36 Transmittance
SP038	CS037	1	Full System Image (FSI) for CS-37	CS37 Transmittance
SP039	CS038	1	Full System Image (FSI) for CS-38	CS38 Transmittance
SP040	CS039	1	Full System Image (FSI) for CS-39	CS39 Transmittance
SP041	CS040	1	Full System Image (FSI) for CS-40	CS40 Transmittance
SP042	CS041	1	Full System Image (FSI) for CS-41	CS41 Transmittance
SP043	CS042	1	Full System Image (FSI) for CS-42	CS42 Transmittance
SP044	CS043	1	Full System Image (FSI) for CS-43	CS43 Transmittance
SP045	CS044	1	Full System Image (FSI) for CS-44	CS44 Transmittance
SP046	CS045	1	Full System Image (FSI) for CS-45	CS45 Transmittance
SP047	CS046	1	Full System Image (FSI) for CS-46	CS46 Transmittance
SP048	CS047	1	Full System Image (FSI) for CS-47	CS47 Transmittance
SP049	CS048	1	Full System Image (FSI) for CS-48	CS48 Transmittance
SP050	CS049	1	Full System Image (FSI) for CS-49	CS49 Transmittance
SP051	CS050	1	Full System Image (FSI) for CS-50	CS50 Transmittance
SP052	CS051	1	Full System Image (FSI) for CS-51	CS51 Transmittance
SP053	CS052	1	Full System Image (FSI) for CS-52	CS52 Transmittance
SP054	CS053	1	Full System Image (FSI) for CS-53	CS53 Transmittance
SP055	CS054	1	Full System Image (FSI) for CS-54	CS54 Transmittance
SP056	CS055	1	Full System Image (FSI) for CS-55	CS55 Transmittance
SP057	CS056	1	Full System Image (FSI) for CS-56	CS56 Transmittance
SP058	CS057	1	Full System Image (FSI) for CS-57	CS57 Transmittance
SP059	CS058	1	Full System Image (FSI) for CS-58	CS58 Transmittance
SP060	CS059	1	Full System Image (FSI) for CS-59	CS59 Transmittance
SP061	CS060	1	Full System Image (FSI) for CS-60	CS60 Transmittance
SP062	CS061	1	Full System Image (FSI) for CS-61	CS61 Transmittance
SP063	CS062	1	Full System Image (FSI) for CS-62	CS62 Transmittance
SP064	CS063	1	Full System Image (FSI) for CS-63	CS63 Transmittance
SP065	CS064	1	Full System Image (FSI) for CS-64	CS64 Transmittance
SP066	CS065	1	Full System Image (FSI) for CS-65	CS65 Transmittance
SP067	CS066	1	Full System Image (FSI) for CS-66	CS66 Transmittance
SP068	CS067	1	Full System Image (FSI) for CS-67	CS67 Transmittance
SP069	CS068	1	Full System Image (FSI) for CS-68	CS68 Transmittance
SP070	CS069	1	Full System Image (FSI) for CS-69	CS69 Transmittance

[illegible]

GPO Number	GPO Name	NO	Functional Description	NO Termination
01001	01001	1/0	Catalytic Over Temperature	100 kΩ pull-up to T12_A0



FBVDDQ_MEM



GD3-256		GD3-256		Channel 1 32.63	
CM00	CAS*	CM016	CAS*		
CM01	CKE	CM017	CKE		
CM02	RST*	CM018	RST*		
CM03	RAS*	CM019	RAS*		
CM04	A1_A9	CM020	A1_A9		
CM05	A0_A10	CM021	A0_A10		
CM06	A17_RFU	CM022	A17_RFU		
CM07	AB*	CM023	AB*		
CM08	AB_A11	CM024	AB_A11		
CM09	A7_A8	CM025	A7_A8		
CM010	WB*	CM026	WB*		
CM011	AS_BA1	CM027	AS_BA1		
CM012	A4_BA2	CM028	A4_BA2		
CM013	A7_BA0	CM029	A7_BA0		
CM014	A3_BA3	CM030	A3_BA3		
CM015	C5*	CM031	C5*		

GD3-256		Channel 0 & 1	
CM032	Hot used		
CM033	Hot used		
CM034	DEBUG*		
CM035	DEBUG*		

Notes:

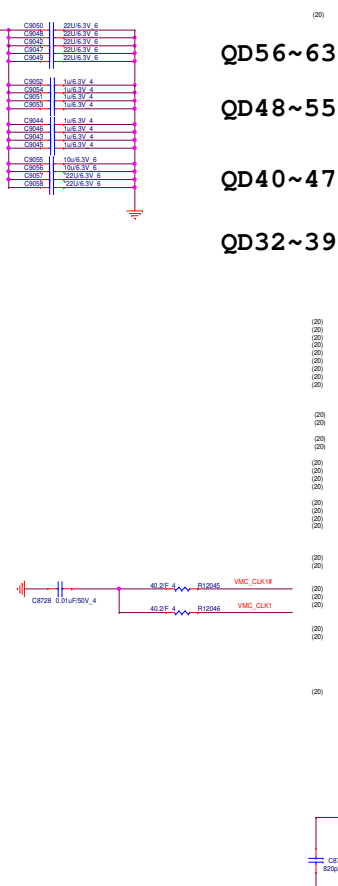
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

Channel 1
<0-31>

MF=0 Non-mirrored

Channe
<0-31>

MF=0 Non-mirrored



CA3-256		Channel 0 D 0, 31	CA3-256	Channel 1 32, 63
CM00	CAS*	CM07	CAS*	
CM01	CKE	CM07	CKE	
CM02	RST*	CM08	RST*	
CM03	BA5*	CM09	BA5*	
CM04	A1_A9	CM00	A1_A9	
CM05	A0_A10	CM01	A0_A10	
CM06	A12_RFU	CM02	A12_RFU	
CM07	AB*	CM03	AB*	
CM08	AB_A11	CM04	AB_A11	
CM09	AB_A8	CM05	AB_A8	
CM00	WE*	CM06	WE*	
CM01	AS_BA1	CM07	AS_BA1	
CM02	AB_BA2	CM08	AB_BA2	
CM03	A2_BA8	CM09	A2_BA8	
CM04	A3_BA3	CM00	A3_BA3	
CM05	CS*	CM03	CS*	

GB3-256		Channel 0 & 1
CM00	Hot User8	
CM01	Hot User8	
CM04	DEBIO*	
CM08	DEBIO*	

1. **Notes:**
 a. GPU debug pins not connected to DBAM. See section 7.1.13.

Notes:
1. GPU debug pins: not connected to DRAM. See section 7.1.13.

Channel 0
<0~31>

MF=1 mirrored

QD0~7

QD8~15

QD16~23

QD24~31

VMD_QD0
VMD_QD1
VMD_QD2
VMD_QD3
VMD_QD4
VMD_QD5
VMD_QD6
VMD_QD7
VMD_QD8
VMD_QD9
VMD_QD10
VMD_QD11
VMD_QD12
VMD_QD13
VMD_QD14
VMD_QD15
VMD_QD16
VMD_QD17
VMD_QD18
VMD_QD19
VMD_QD20
VMD_QD21
VMD_QD22
VMD_QD23
VMD_QD24
VMD_QD25
VMD_QD26
VMD_QD27
VMD_QD28
VMD_QD29
VMD_QD30
VMD_QD31

FBD_CMD6
FBD_CMD7
FBD_CMD8
FBD_CMD9
FBD_CMD10
FBD_CMD11
FBD_CMD12
FBD_CMD13
FBD_CMD14

VMD_WCK23
VMD_WCK24
VMD_WCK25
VMD_WCK26

FBD_EDC0
FBD_EDC1
FBD_EDC2
FBD_EDC3

FBD_DBI0
FBD_DBI1
FBD_DBI2
FBD_DBI3

FBD_CMD0
FBD_CMD1

FBD_CMD2
FBD_CMD3
FBD_CMD4
FBD_CMD5

SEN_D0
FBD_CMD2

DBIT_D41

FBD_VREFC
FBD_CMD7

MEM_VREF_CTL_OD

MEM_VREF_CTL

Channel 1
<0~31>

MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

VMD_QD56
VMD_QD57
VMD_QD58
VMD_QD59
VMD_QD60
VMD_QD61
VMD_QD62
VMD_QD63
VMD_QD64
VMD_QD65
VMD_QD66
VMD_QD67
VMD_QD68
VMD_QD69
VMD_QD70
VMD_QD71
VMD_QD72
VMD_QD73
VMD_QD74
VMD_QD75
VMD_QD76
VMD_QD77
VMD_QD78
VMD_QD79
VMD_QD80
VMD_QD81
VMD_QD82
VMD_QD83
VMD_QD84
VMD_QD85
VMD_QD86
VMD_QD87
VMD_QD88
VMD_QD89
VMD_QD90
VMD_QD91
VMD_QD92
VMD_QD93
VMD_QD94
VMD_QD95
VMD_QD96
VMD_QD97
VMD_QD98
VMD_QD99

FBD_CMD22
FBD_CMD23
FBD_CMD24
FBD_CMD25
FBD_CMD26
FBD_CMD27
FBD_CMD28
FBD_CMD29
FBD_CMD30
FBD_CMD31
FBD_CMD32

VMD_WCK45
VMD_WCK46
VMD_WCK47
VMD_WCK48

FBD_EDC7
FBD_EDC8
FBD_EDC9
FBD_EDC10

FBD_DBI7
FBD_DBI8
FBD_DBI9
FBD_DBI10

FBD_CMD19
FBD_CMD20

FBD_CMD17
FBD_CMD18
FBD_CMD19
FBD_CMD20

SEN_D0
FBD_CMD18

DBIT_D41

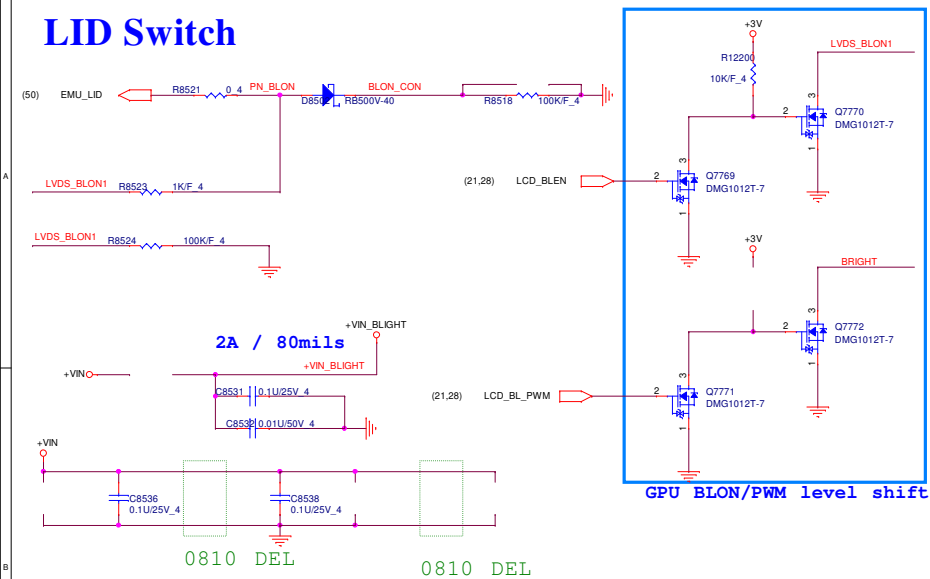
FBD_VREFC
FBD_CMD3

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
Cmd0	CAS*	Cmd16	CAS*
Cmd1	CKE	Cmd17	CKE
Cmd2	RST*	Cmd18	RST*
Cmd3	RAS*	Cmd19	RAS*
Cmd4	A1_A9	Cmd20	A1_A9
Cmd5	A0_A10	Cmd21	A0_A10
Cmd6	A12_R1U	Cmd22	A12_R1U
Cmd7	AB*	Cmd23	AB*
Cmd8	A6_A11	Cmd24	A6_A11
Cmd9	A7_A8	Cmd25	A7_A8
Cmd10	WE*	Cmd26	WE*
Cmd11	A5_BA1	Cmd27	A5_BA1
Cmd12	A4_BA2	Cmd28	A4_BA2
Cmd13	A7_BA8	Cmd29	A7_BA8
Cmd14	A3_BA3	Cmd30	A3_BA3
Cmd15	C3*	Cmd31	C3*
GB3-256 Channel 0 & 1			
Cmd32	Not used		
Cmd33	Not used		
Cmd34	DEBUG0		
Cmd35	DEBUG1		

Notes:
1. GPU debug pins: not connected to DRAM, see section 7.1.13.

LID Switch



```
0809  add
```

```
0818 add CPU output
```

Reserve for Touch screen

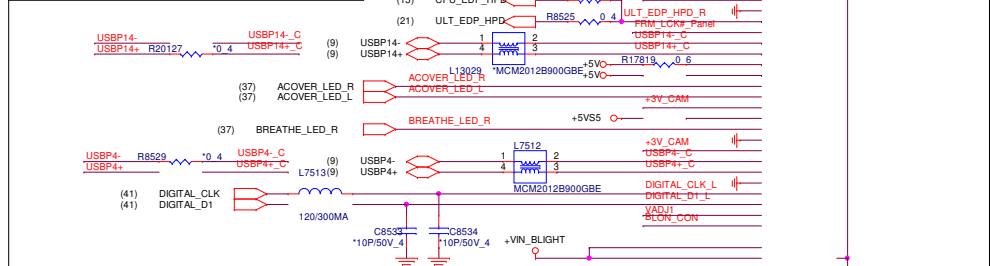
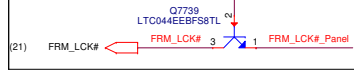
0719 Delete TS

eDP Conn.

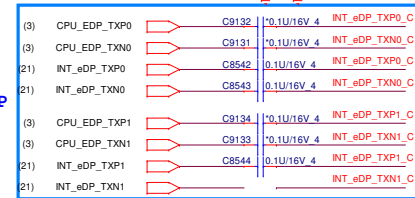
0816 Del

2.5A / 100mils

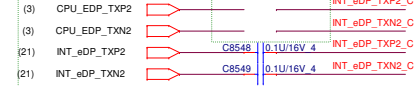
for NVSR(Gsync) +3V_LCD_CON



CPU/GPU EDP
co-lay



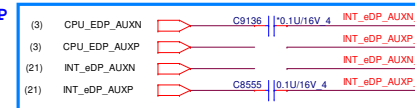
```
PV 1026  umount
[...]:INT 05
```



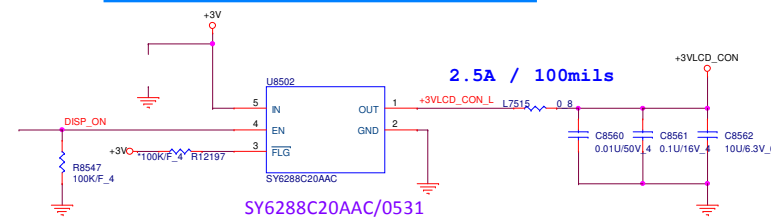
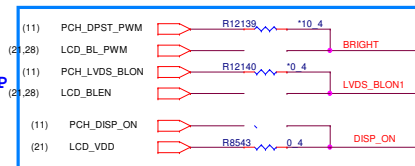
PV 1026 umount



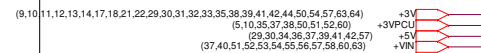
CPU/GPU EDP
co-lay



CPU/GPU EDP
co-lay



SY6288C20AAC/0531



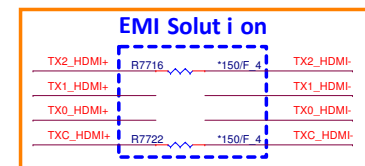
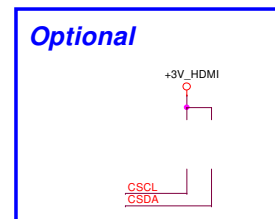
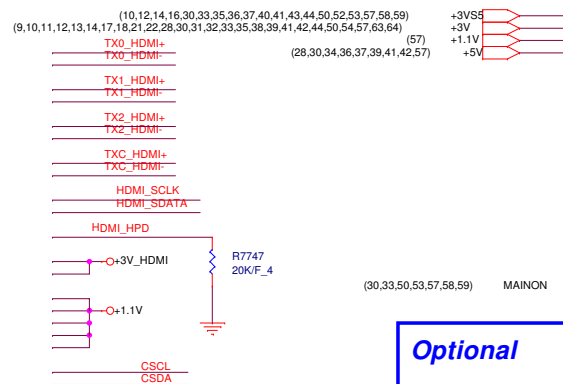
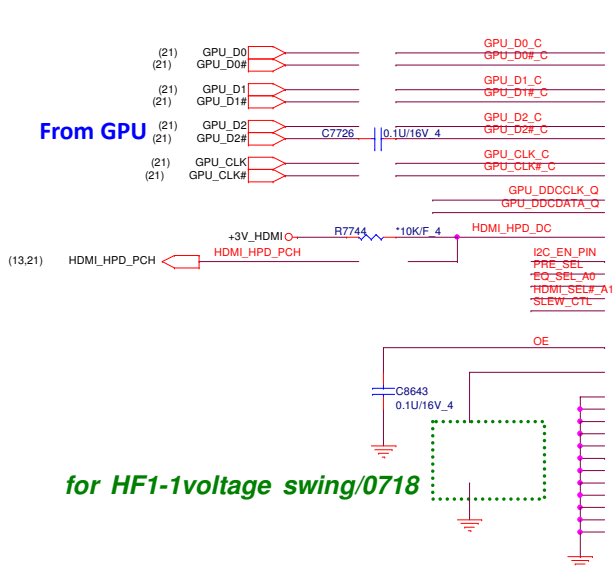
28

0803 Change footprint

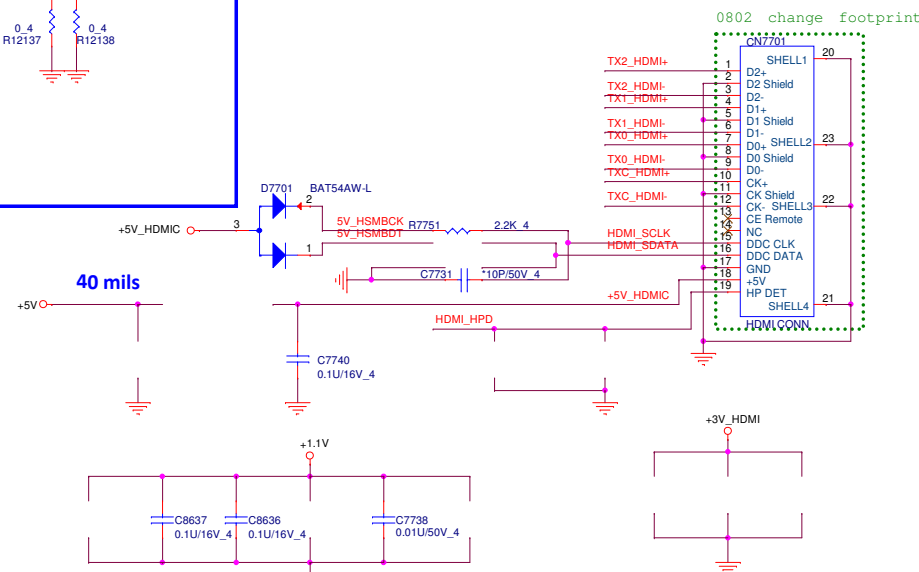
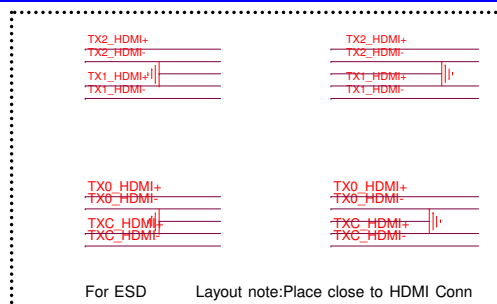
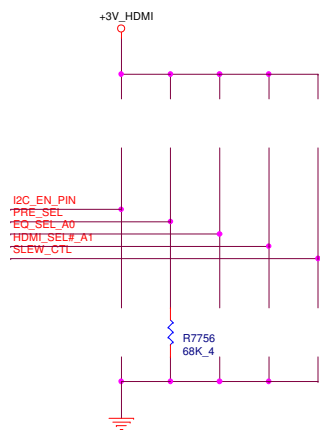
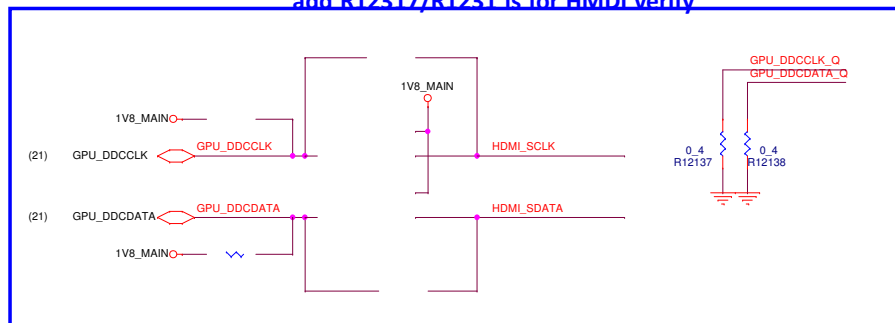
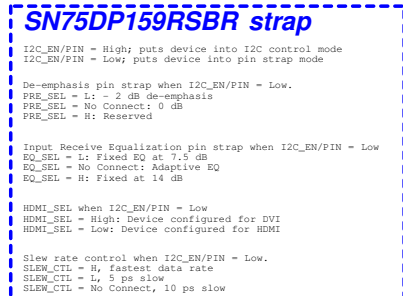
0810 DEL

follow NV
suggest_0303

add the pull high/0602



Prevent current leakage when GPU is power of f
add R12317/R1231 is for HDMI verify

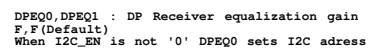




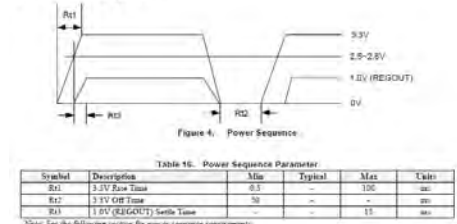
Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	BP_FSW



```
I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable) (Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V
```



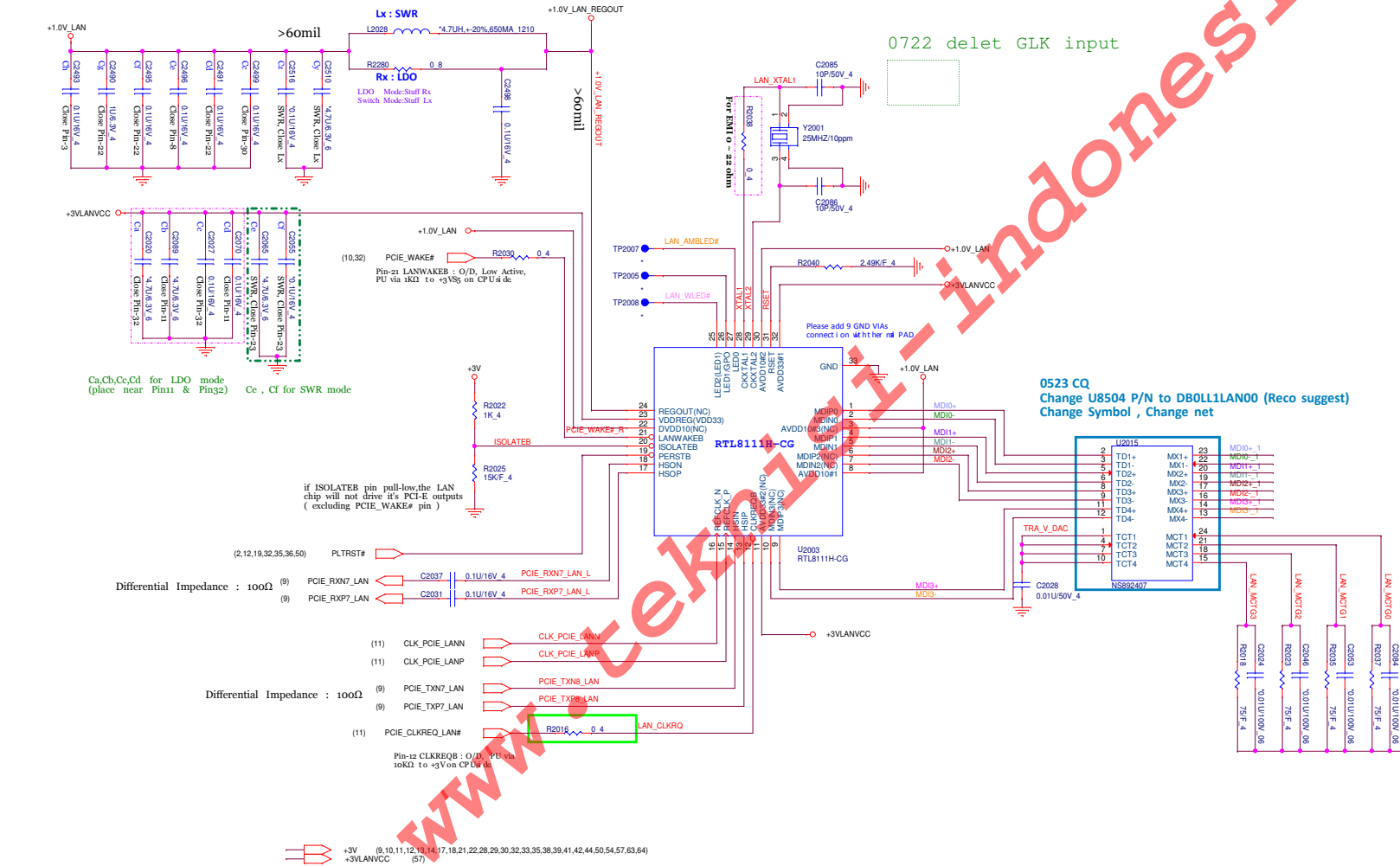
9. Power Sequence



Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Ch close to each VDD10 pin22

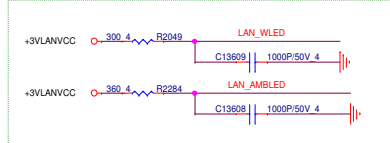
Power trace Layout W > 60mil
Trace<30 mil
Width > 60 mil

RTL8111HS (SWR Mode) Pin-24 REGOUT : Switching Regulator 1.0V Output.
RTL8111H (LDO Mode) Pin-24 REGOUT : LDO Regulator 1.0V Output.

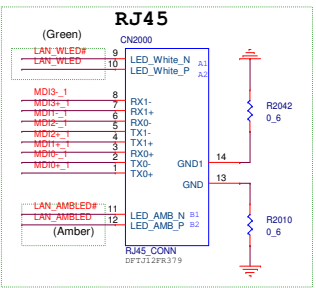


0722 delet GLK input

0803 modify



LAN CONN

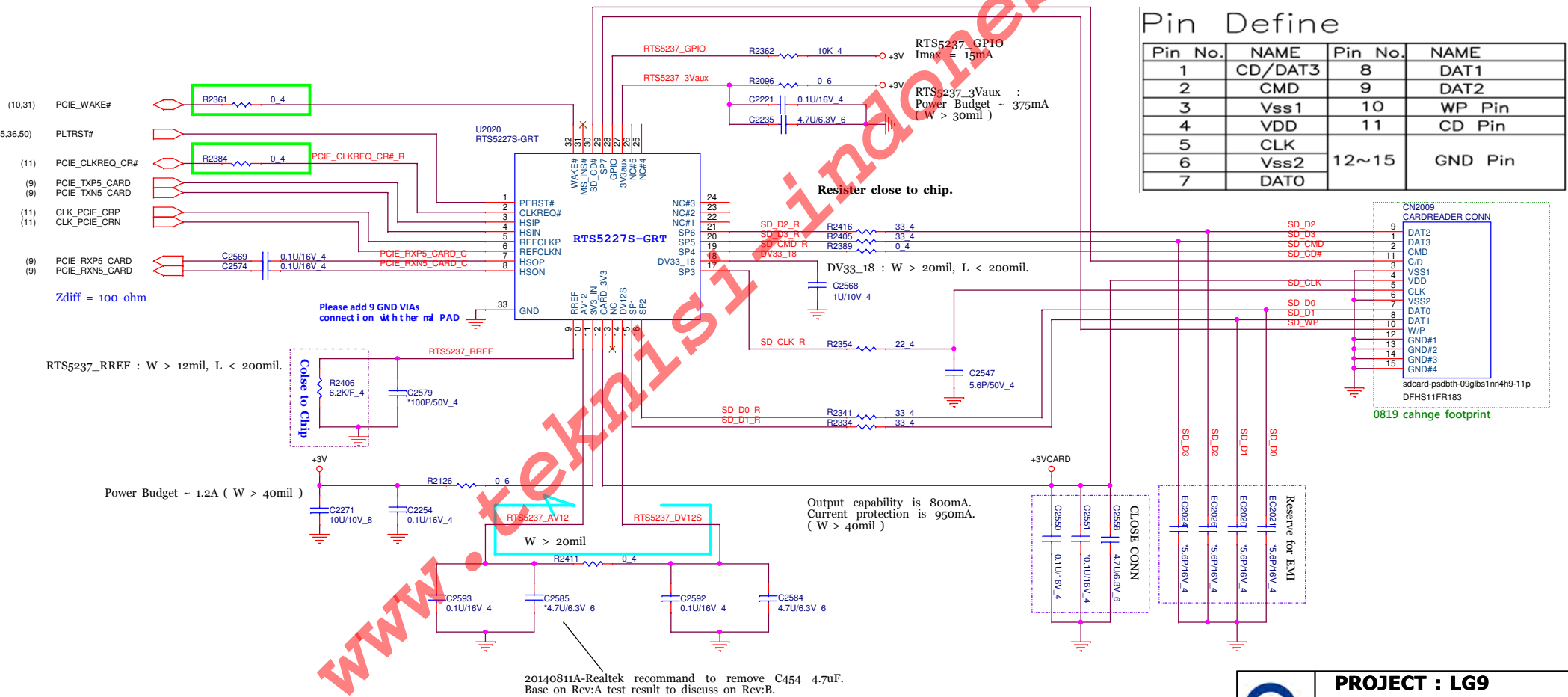


0825 modify

0825 modify

0803 change footprint

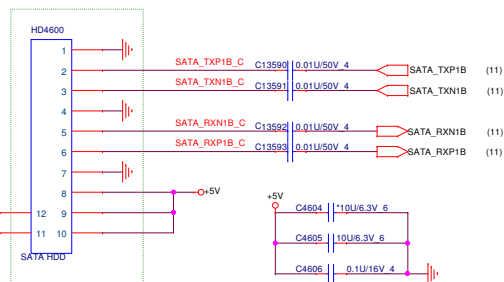
RTL8111GS : Switching Regulator
RTL8111G : LDO Regulator



PROJECT : LG9
Quanta Computer Inc.

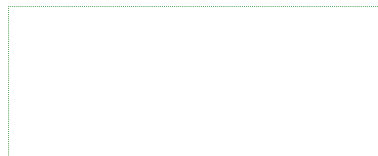
Customer: TPM / Card Reader	Document Number	1A Rev
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Date:	Sheet	of

HDD



0825 Swap pin

0722 delete SATA redriver IC



(9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35,38,39,41,42,44,50,54,57,63,64)
(28,29,30,36,37,39,41,42,57)
(5,10,35,37,38,50,51,52,60)

+3V
+5V
+3VPCU

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0718 delete 3D CAM

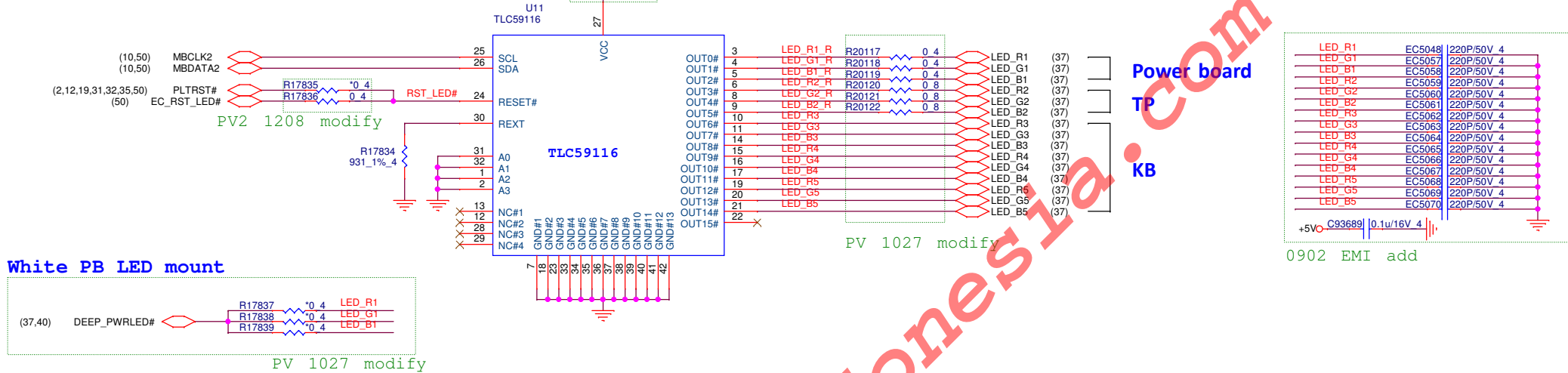


(22,58,64) +1.8V



RGB KB LED Driver

36

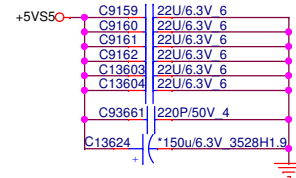
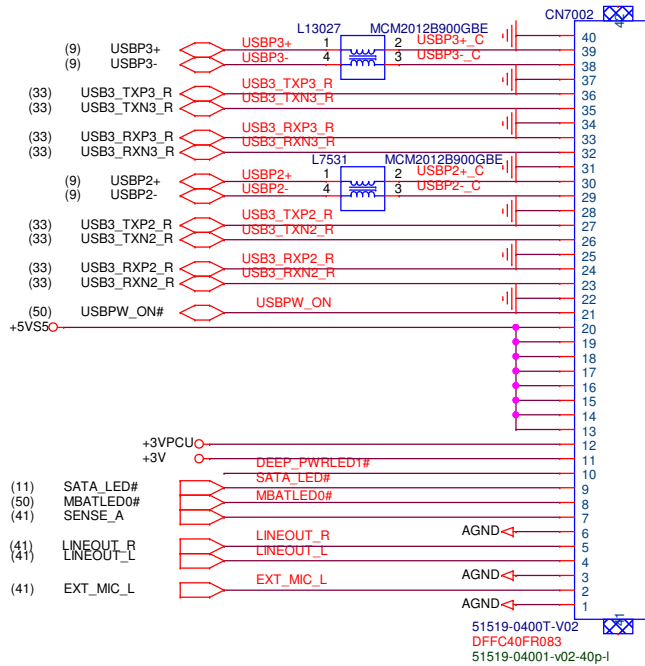


PROJECT : G38A
Quanta Computer Inc.

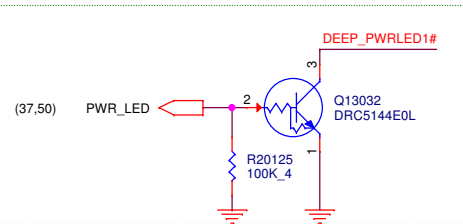
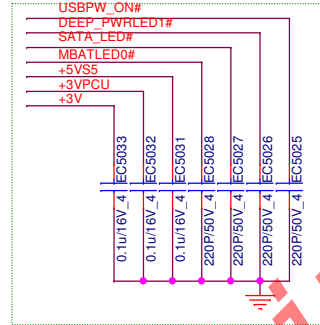
Size	Document Number	Rev
	TPM/G-Sensor/IR CAM	1A
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Daughter Board

0803 change footprint



0807 EMI Stuff



PV 1102 add



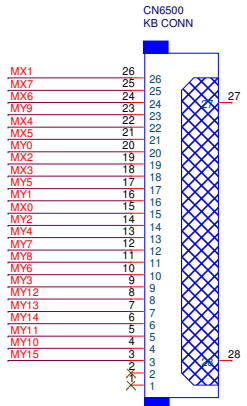
PROJECT : G38A
Quanta Computer Inc.

Size	Document Number	Rev
	TPM/G-Sensor/IR CAM	1A

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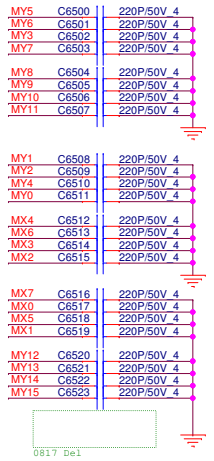
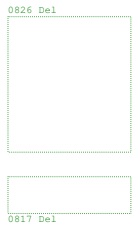
KEYBOARD Con.

(50) MY[0..15] MY[0..15]
(50) MX[0..7] MX[0..7]



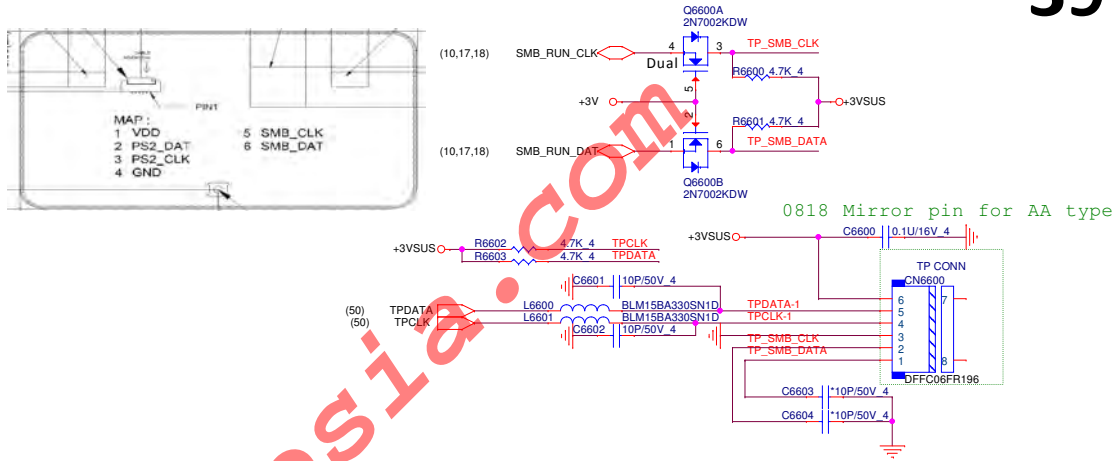
748442605c1-26p-1
DFFC26FR068
0803 change footprint
0817 Modify pin define

KEYBOARD PULL-UP

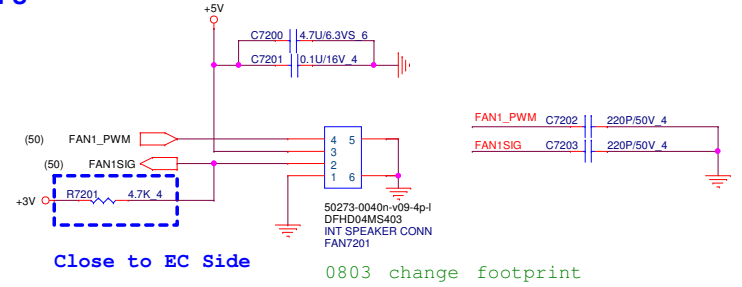


Touch Pad Connector AA type

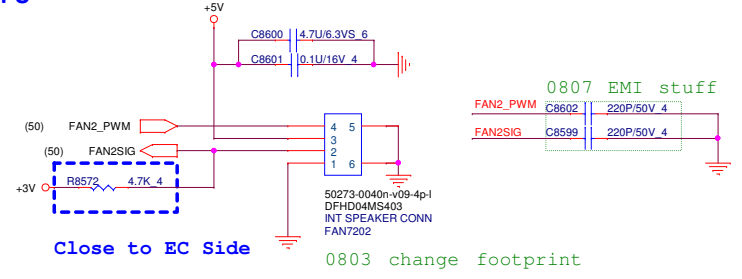
39



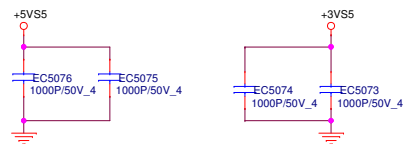
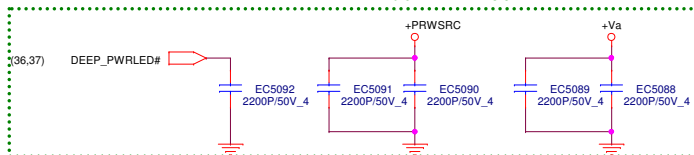
FAN1 for CPU



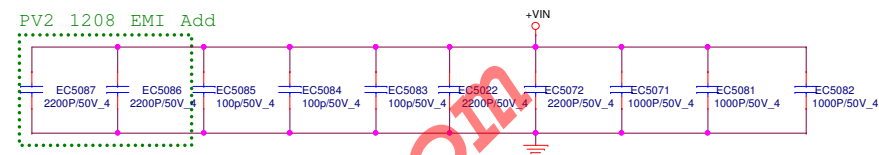
FAN2 for GPU



PV2 1208 EMI Add



PV2 1208 EMI Add

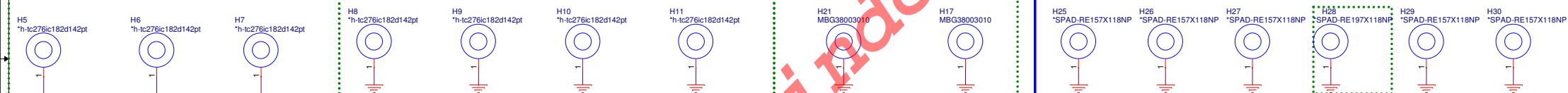


GPU BTK Hole

CPU BTK Hole

WLAN NUT SSD NUT

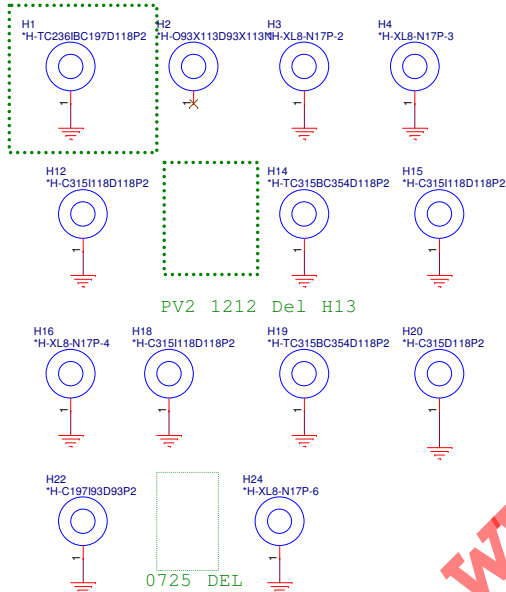
EMI PAD



0909 modify

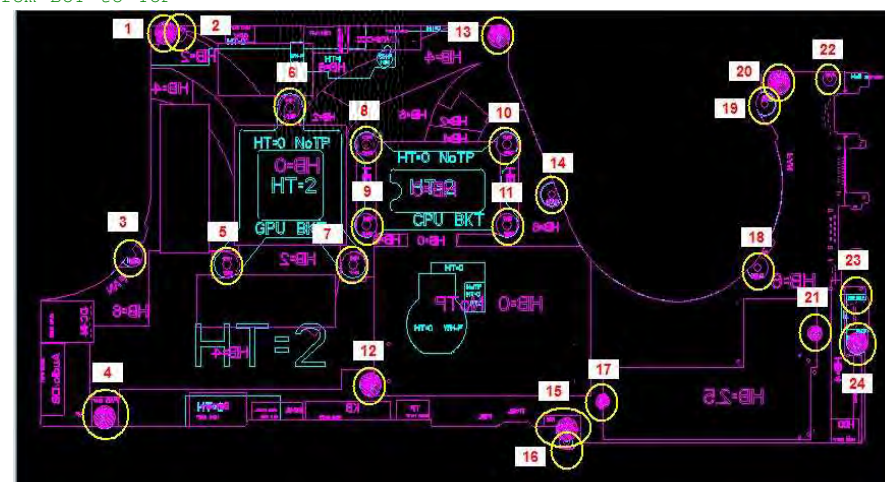
0909 modify


PV 1021 change from BOT to TOP

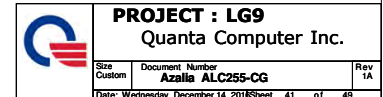


PV2 1212 Del H13

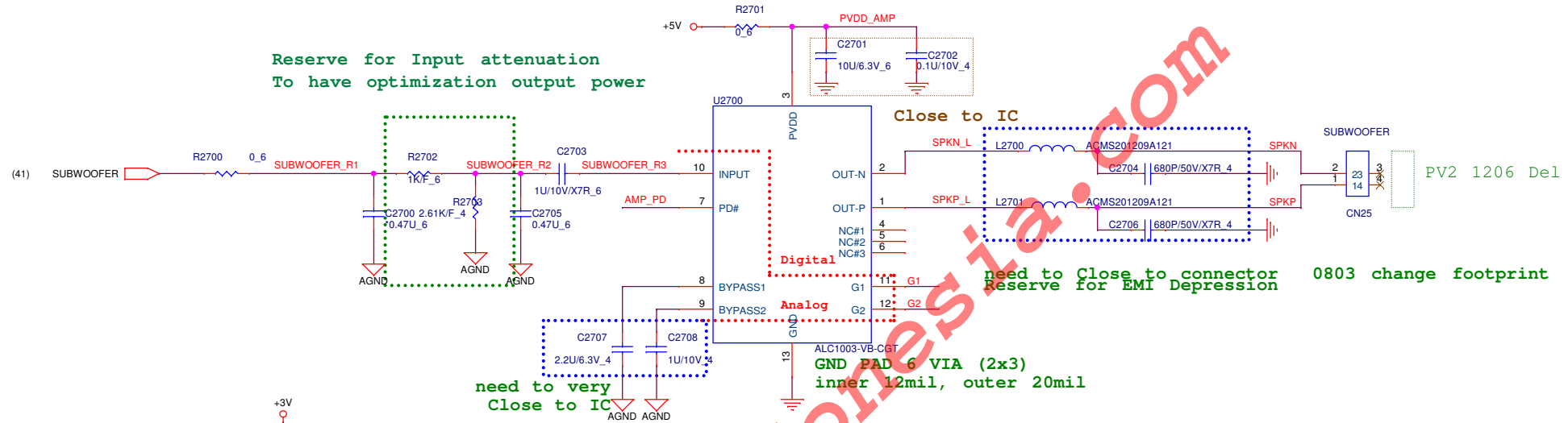
0725 DEL



	PROJECT : G38A		
	Quanta Computer Inc.		
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	RF Solution/HOLE		
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Reserve for Input attenuation
To have optimization output power



Output Gain Table

R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

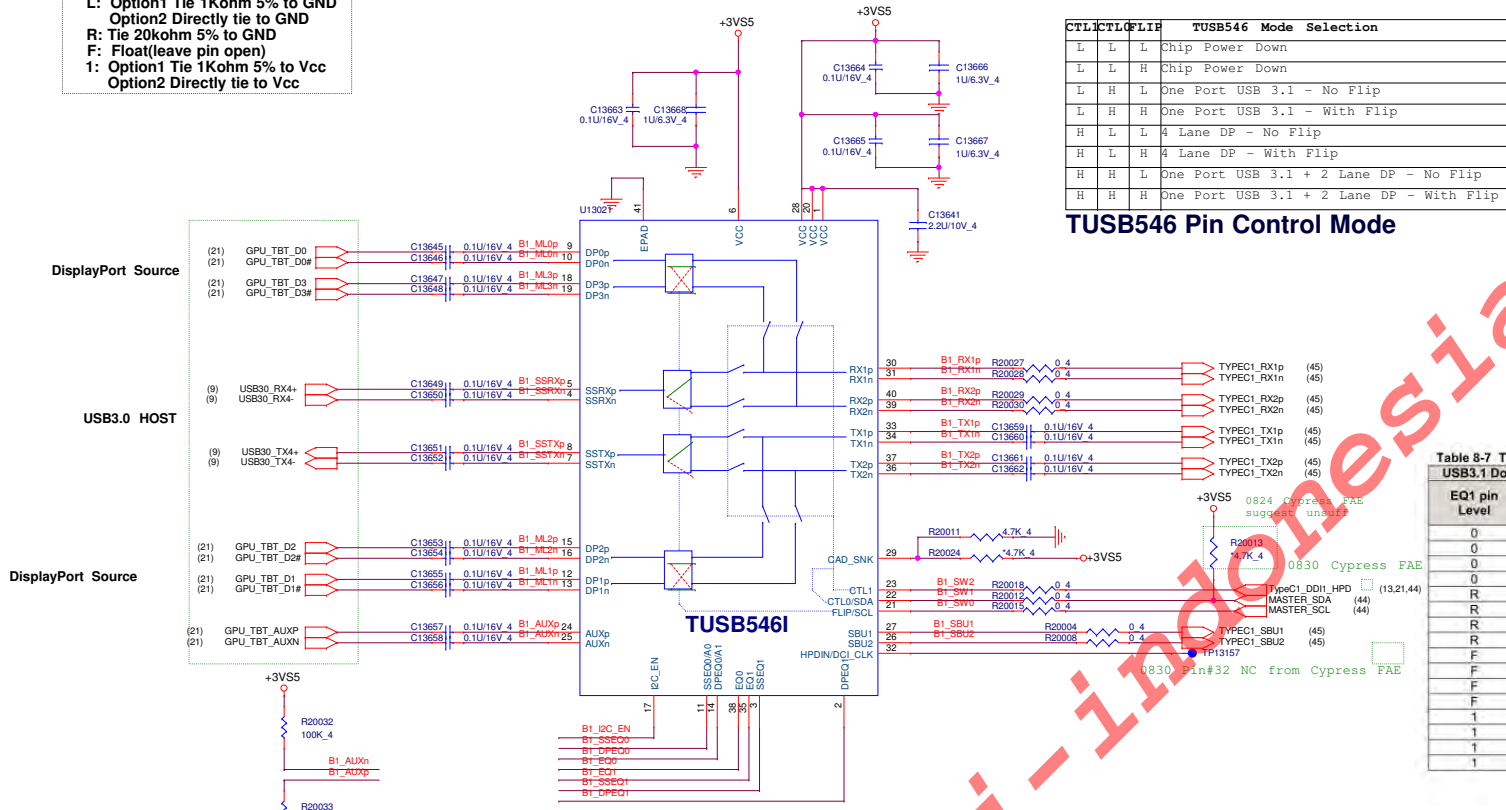


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PROJECT :

Size Custom	Document Number Amplifier(ALC1003)	Rev 3B
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4 Level Input:
L: Option1 Tie 1Kohm 5% to GND
Option2 Directly tie to GND
R: Tie 20kohm 5% to GND
F: Float(leave pin open)
1: Option1 Tie 1Kohm 5% to Vcc
Option2 Directly tie to Vcc



CTL1	CTL2	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

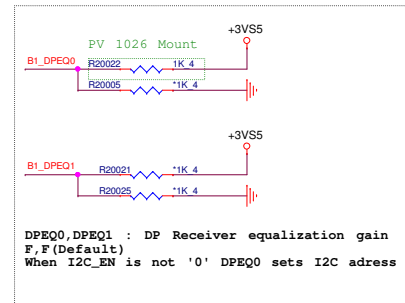
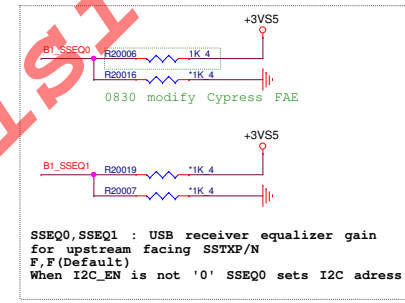
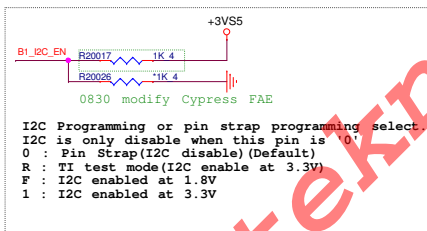
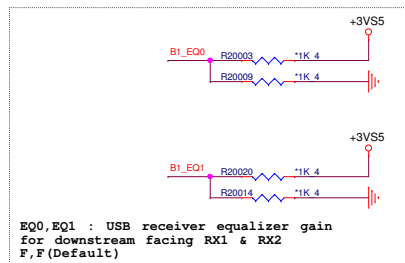
TUSB546 Pin Control Mode

CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L	L	One Port USB 3.1 - No Flip

AUX Pin Control Mode

Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @2.5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @2.5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @2.5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15



CC+PD

0824 add

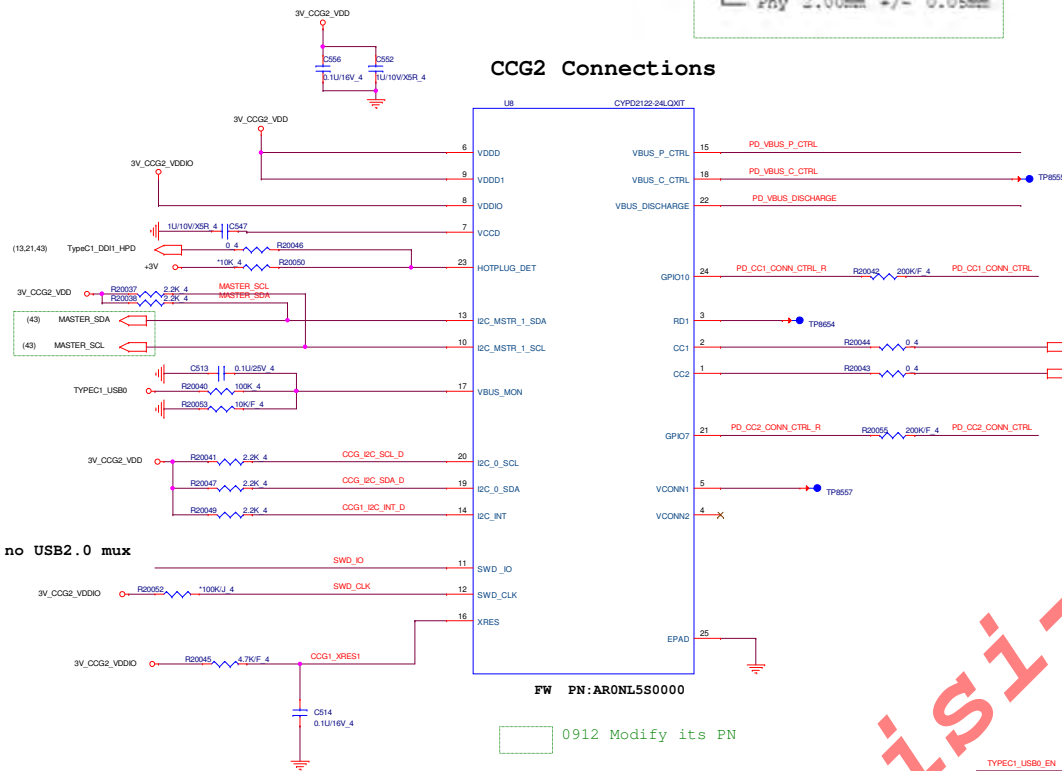
3V_CCG2_VDD
 CCG1_XRES1
 SWD_CLK
 SWD_IO

The Test Points :

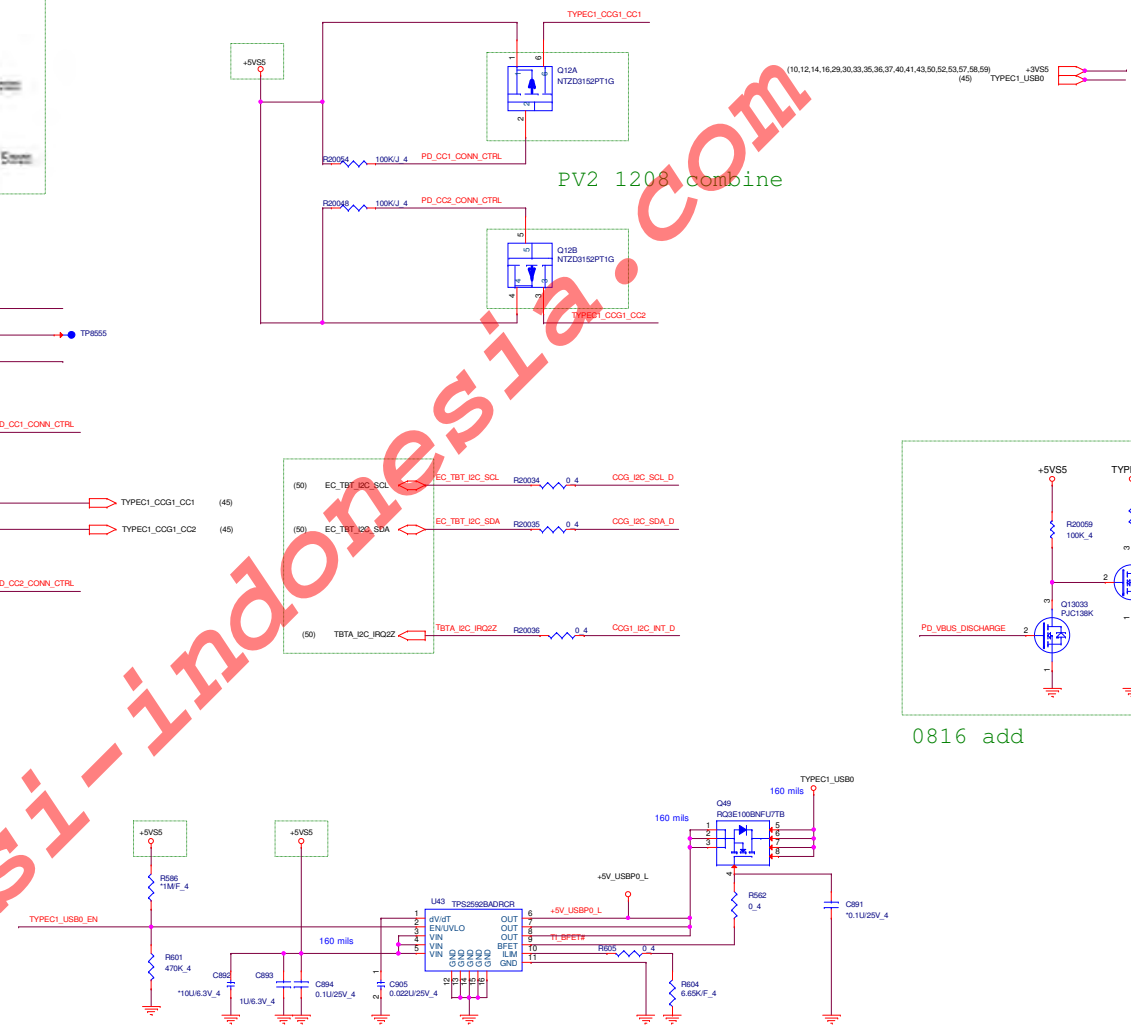
Pitch 2.54mm +/- 0.05mm

Phy 2.00mm +/- 0.05mm

CCG2 Connections

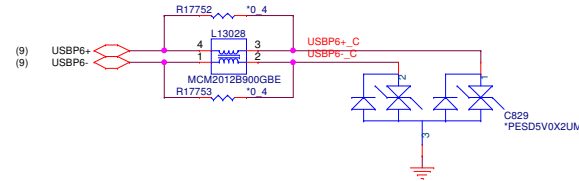


PV2 1208 combine

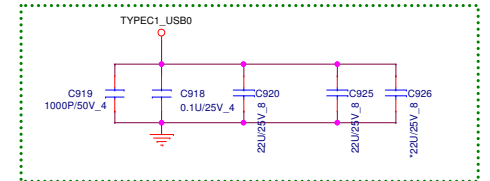
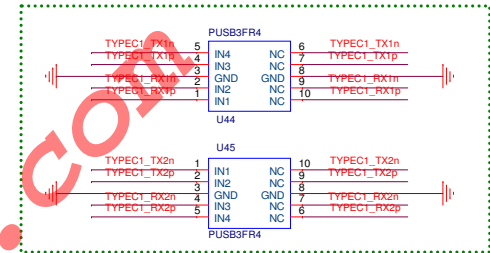


$$R_{lim} = (I_{lim} - 0.7) / (3 * 0.00001)$$

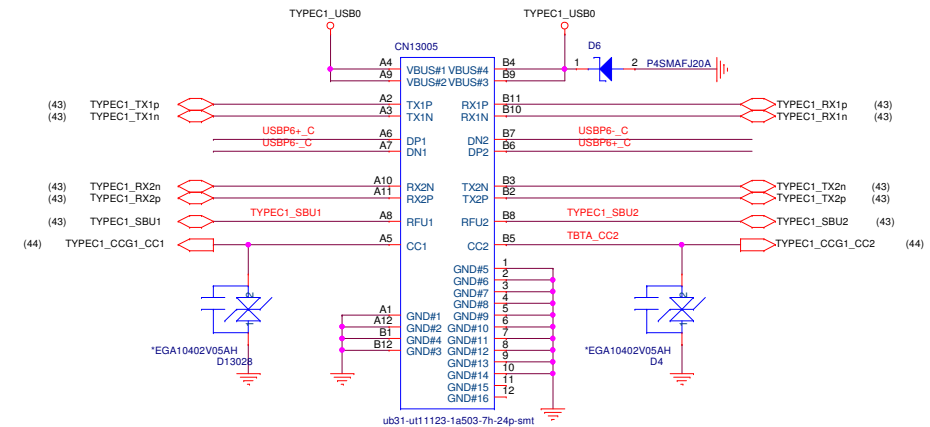
fix 0.9A



Reserve ESD chip



USB Type-C Port A



0802 modify footprint, follow S400

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Quanta Computer Inc.

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NB5

PROJECT : G38A
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 NB5	PROJECT : G38A Quanta Computer Inc.		
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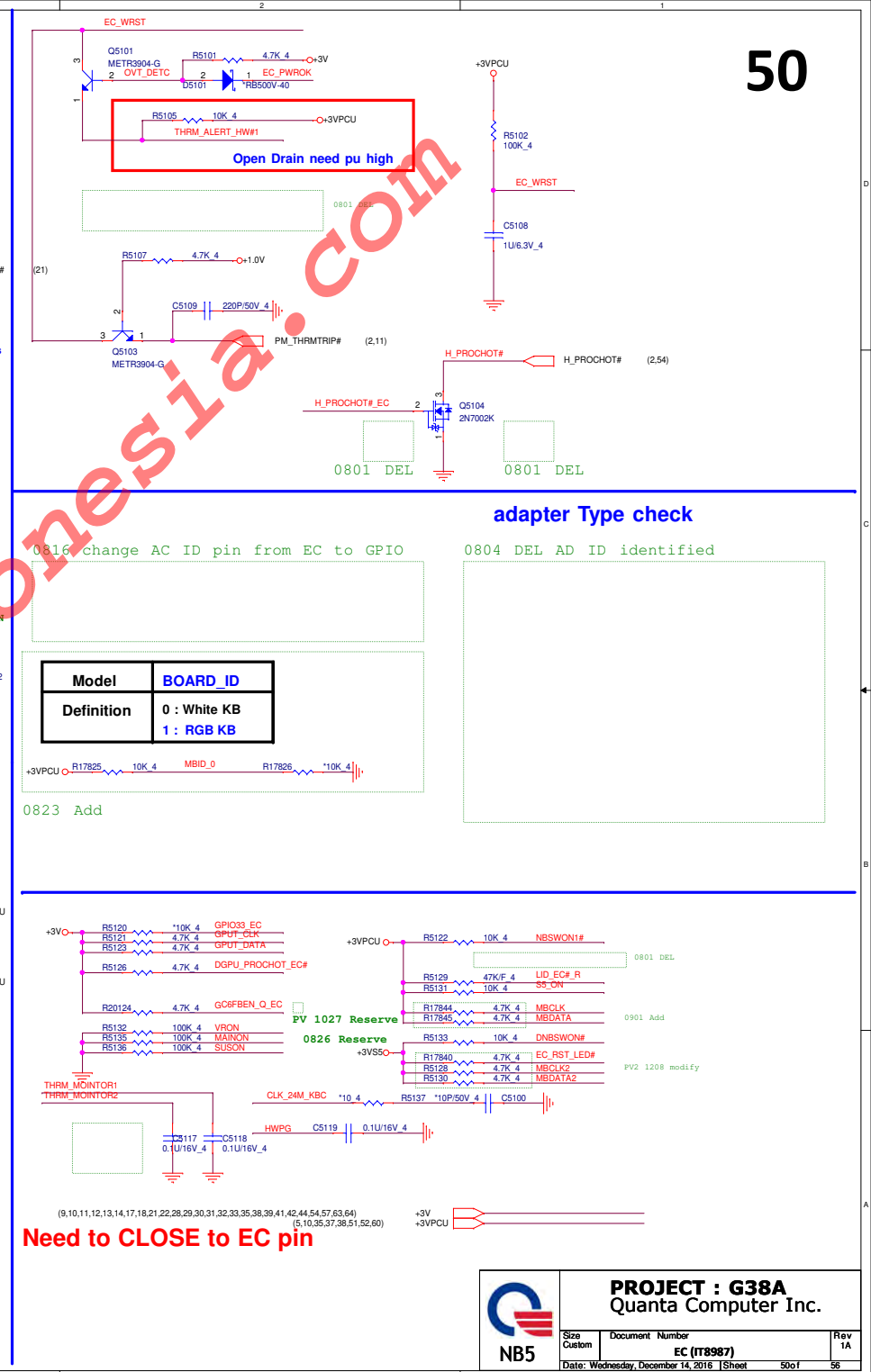
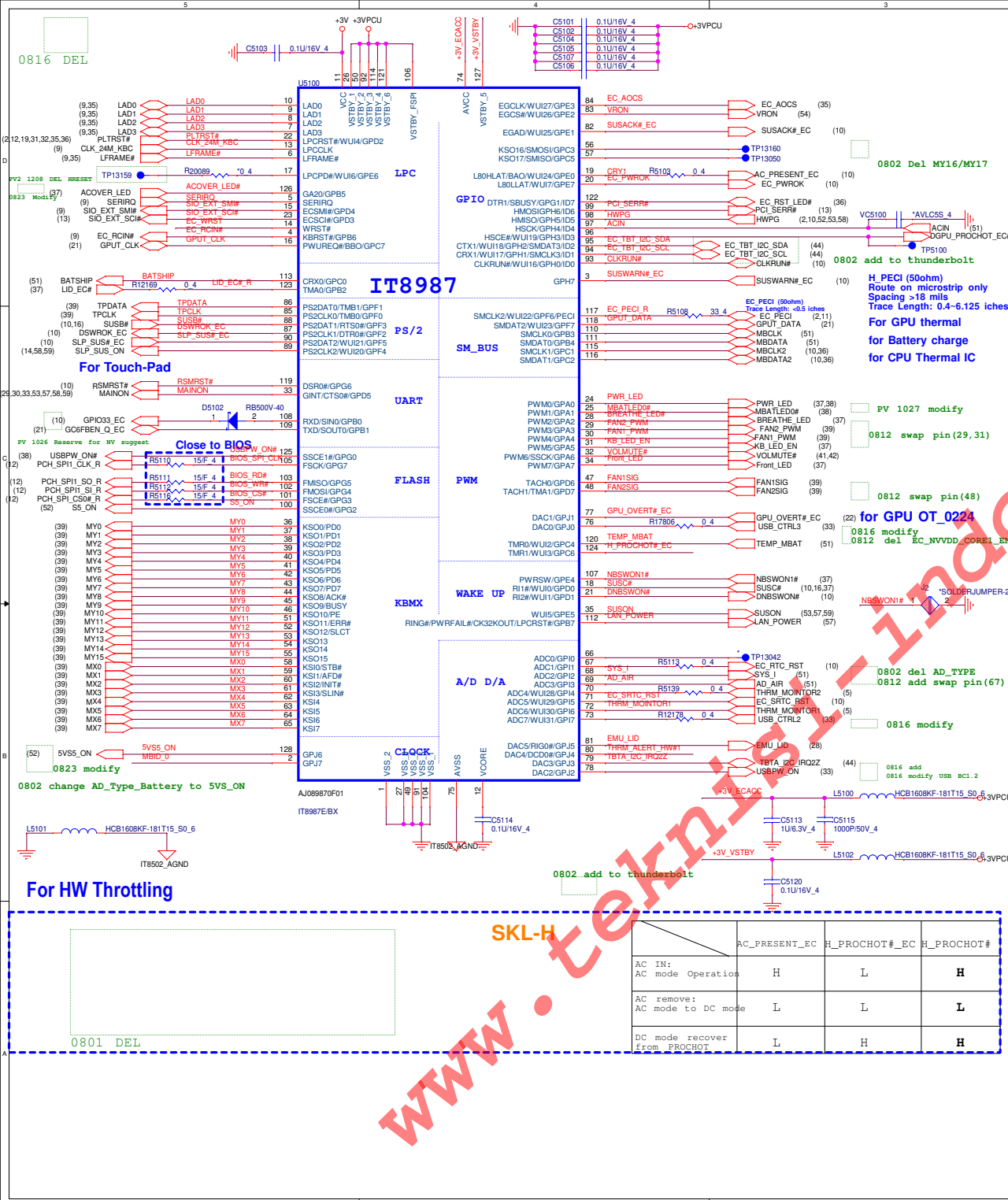
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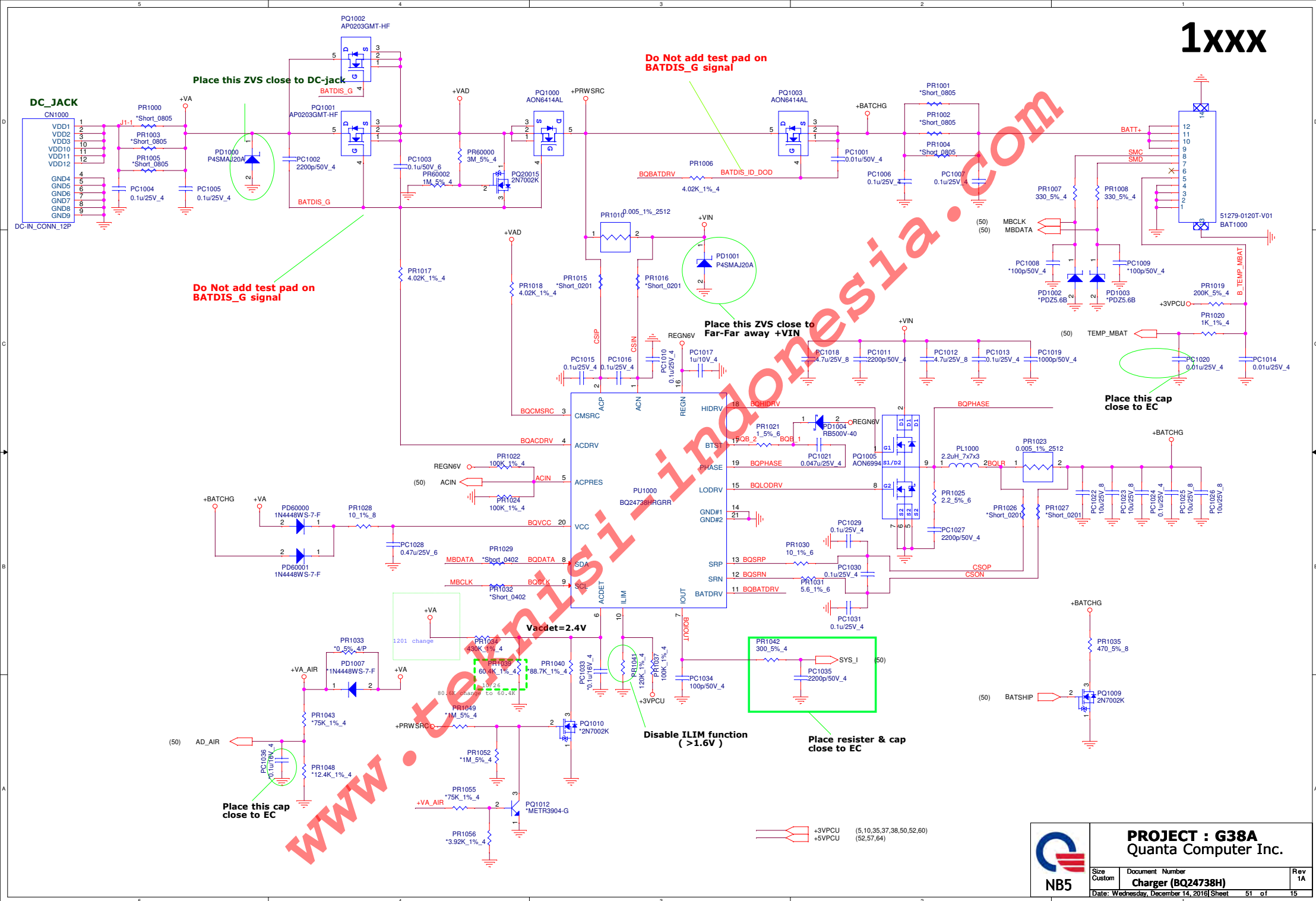
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Size	Document Number TPM/G-Sensor/IR CAM	Rev 1A
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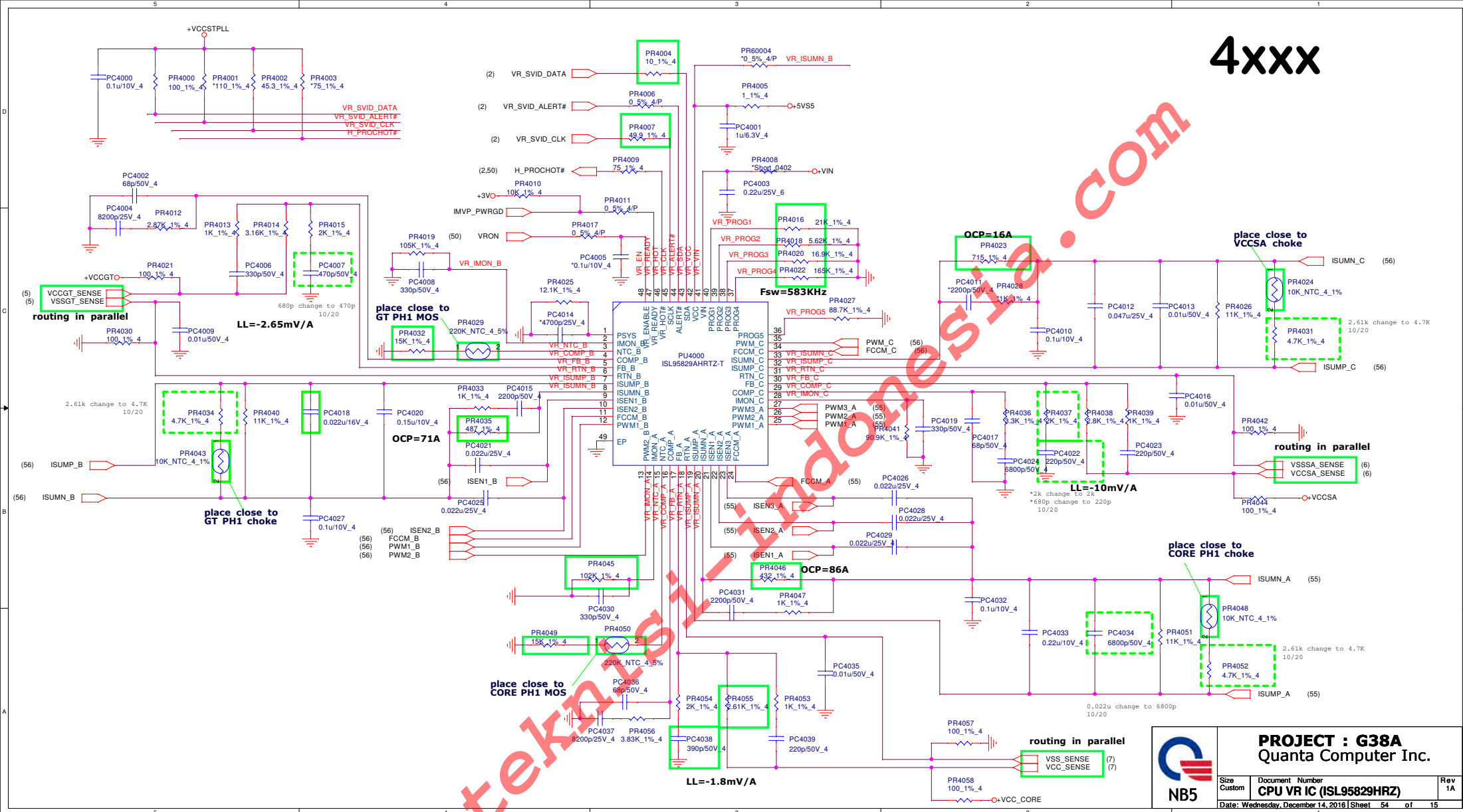



1xxx



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4xxx

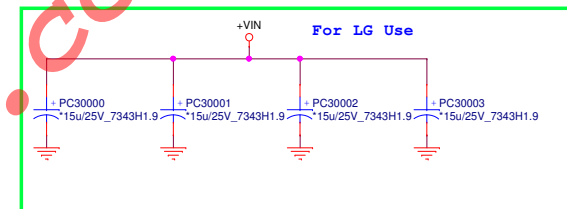
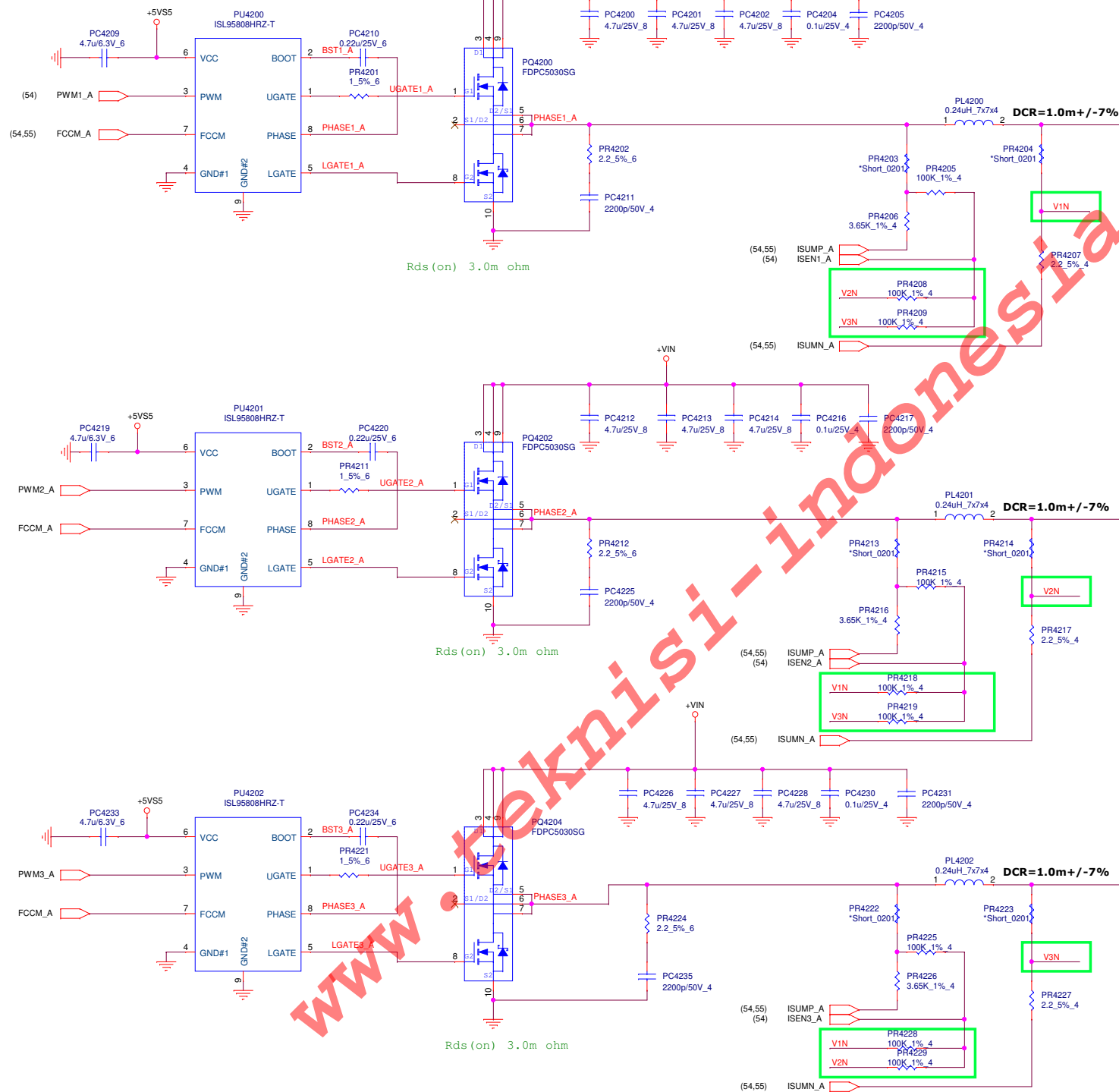




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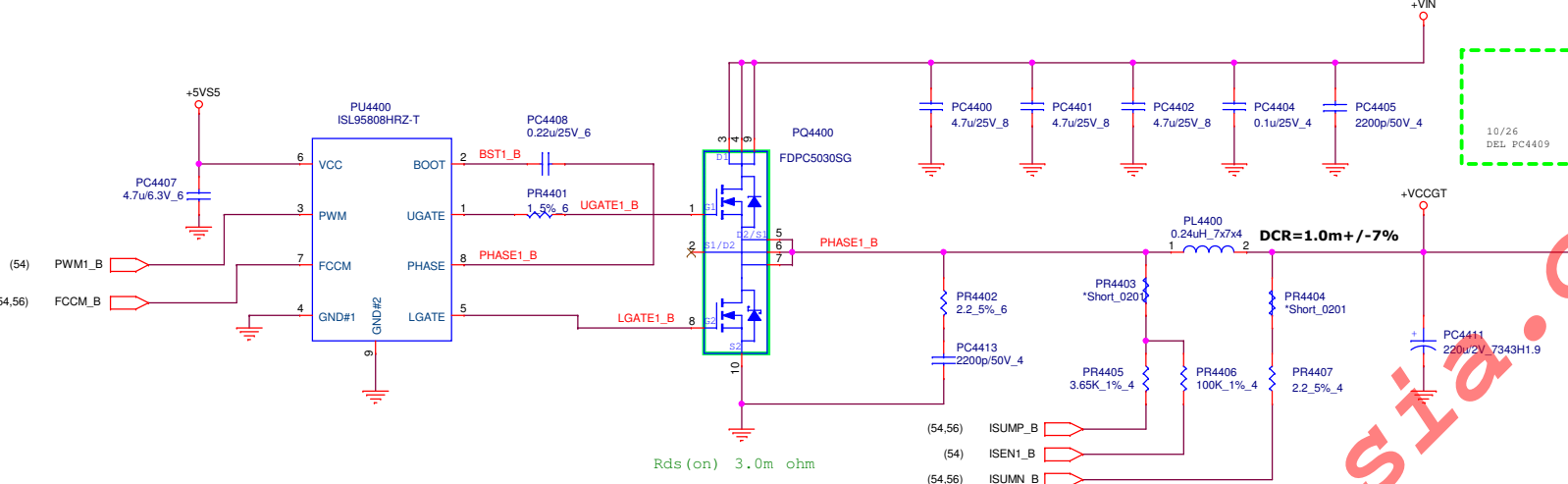
Size	Document Number	Rev
Custom	CPU VR IC (ISL95829HRZ)	1A
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4xxx

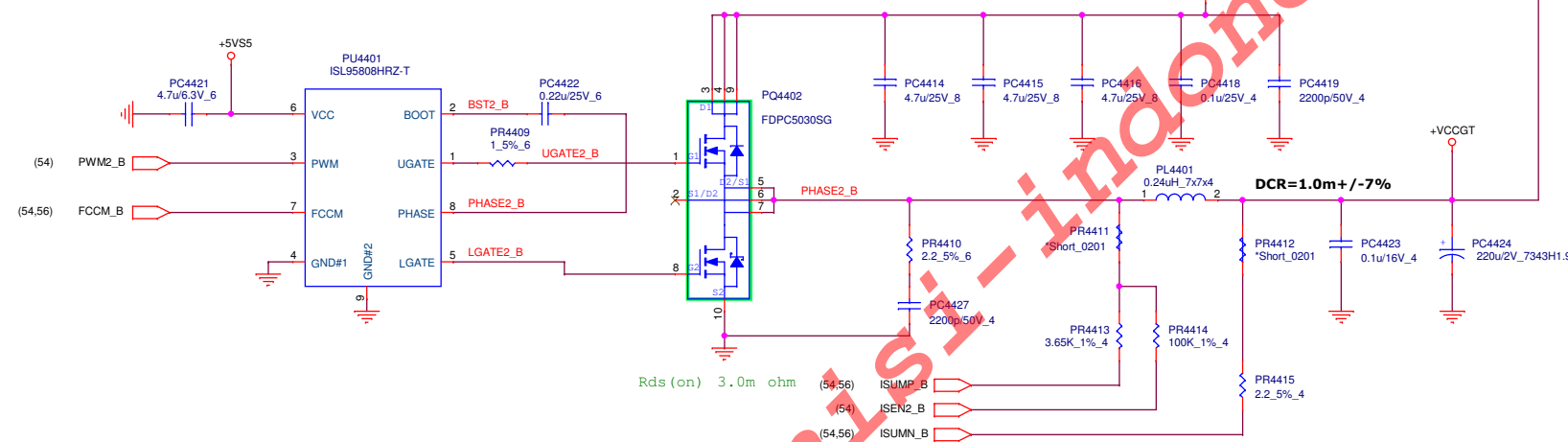


H-line42 (45W)
TDC: 50A
Iccmax: 68A
OCP: 86A
Loadline = -1.8 mV/A

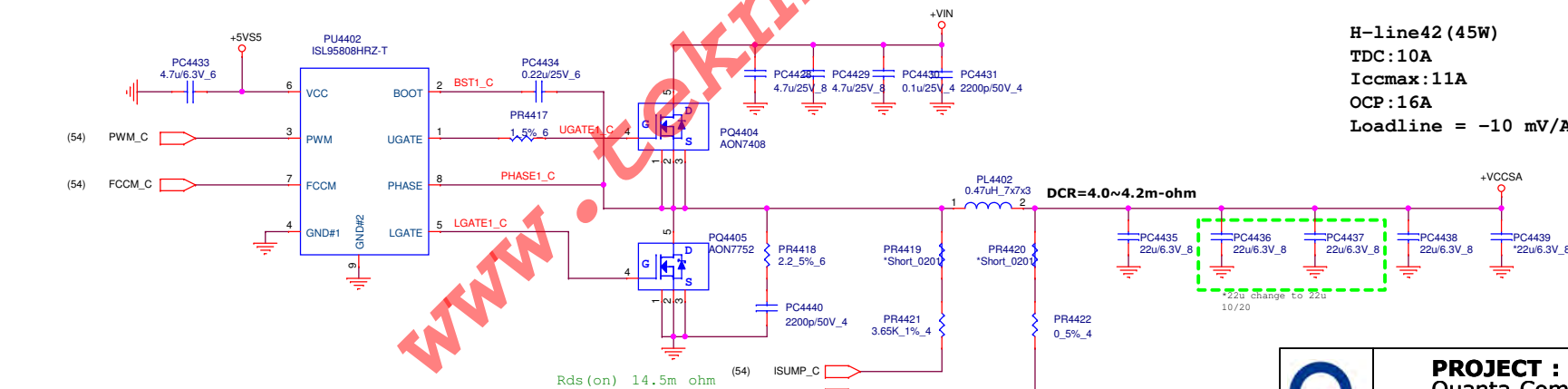
4xxx



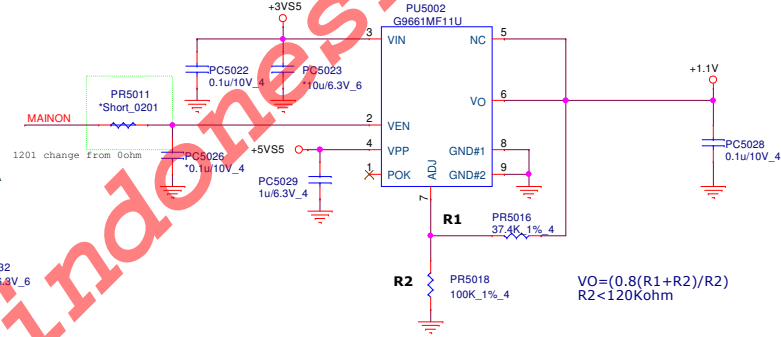
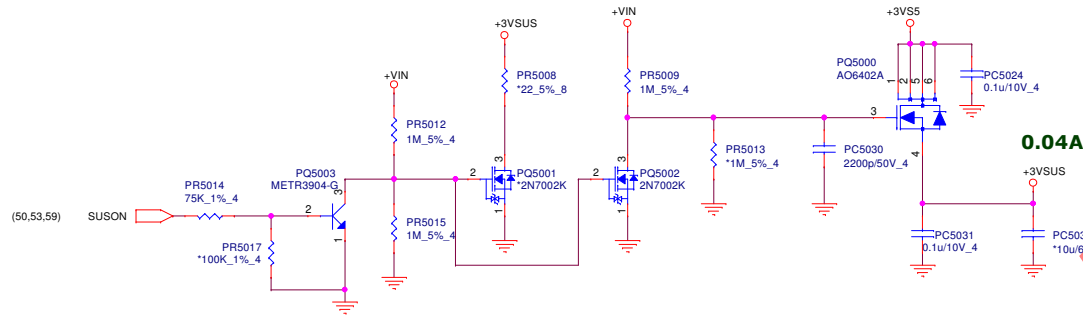
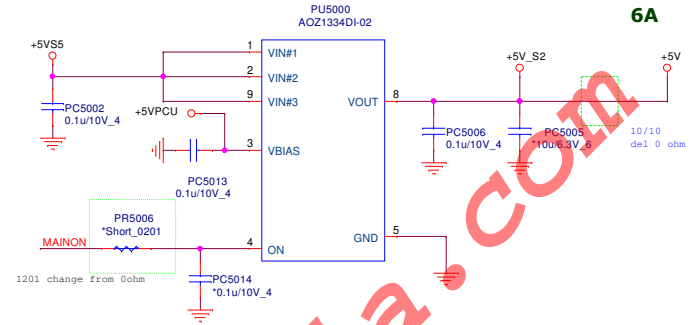
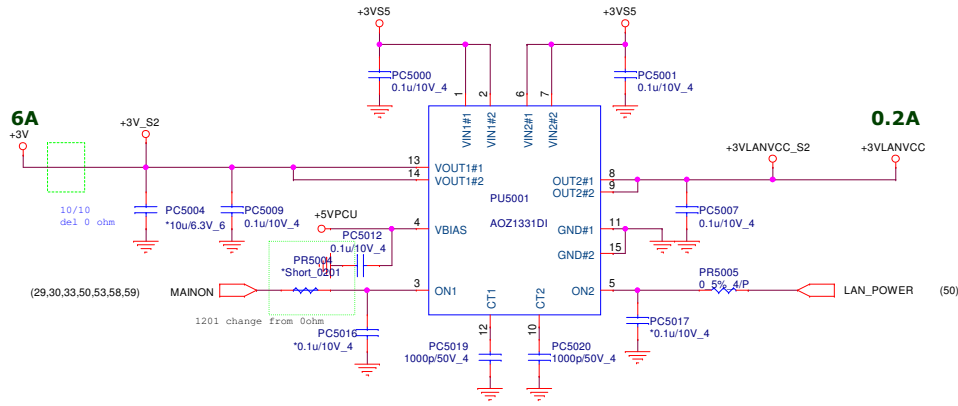
H-line42 (45W)
TDC:25A
Iccmax:55A
OCP:71A
Loadline = -2.65 mV/A



H-line42 (45W)
TDC:10A
Iccmax:11A
OCP:16A
Loadline = -10 mV/A



5xxx



- +3V (9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35,38,39,41,42,44,50,54,63,64)
- +5V (28,29,30,34,36,37,39,41,42)
- +3VS5 (10,12,14,16,29,30,33,35,36,37,40,41,43,44,50,52,53,58,59)
- +5VS5 (10,28,33,37,38,40,44,52,53,54,55,56,58,59,60,61,62,63,64)
- +3VSUS (39)
- +3VLANVCC (31)

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Volume Segment

Vcc_ST: 0.12A

Vcc_PLL: 0.12A

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)

+1.0VS5 Volt +/- 5%

Continue: 6A

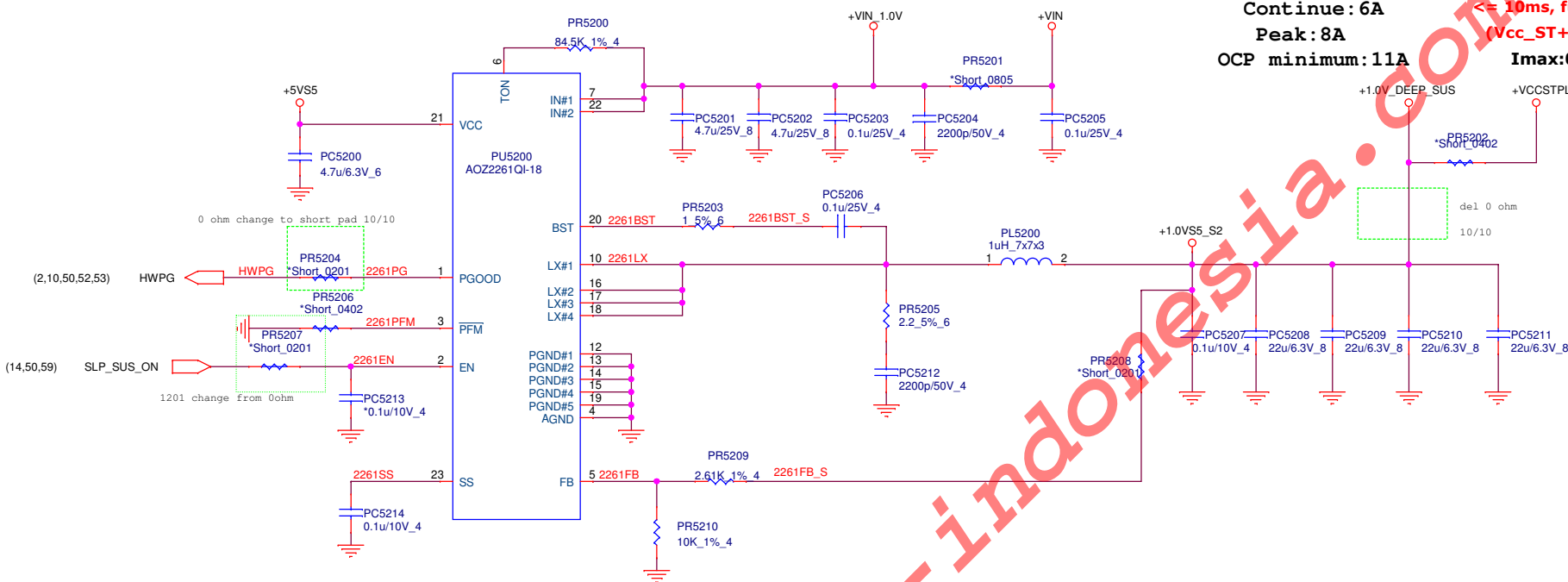
Peak: 8A

OCP minimum: 11A

<= 10ms, full load ready

(Vcc_ST+Vcc_PLL)

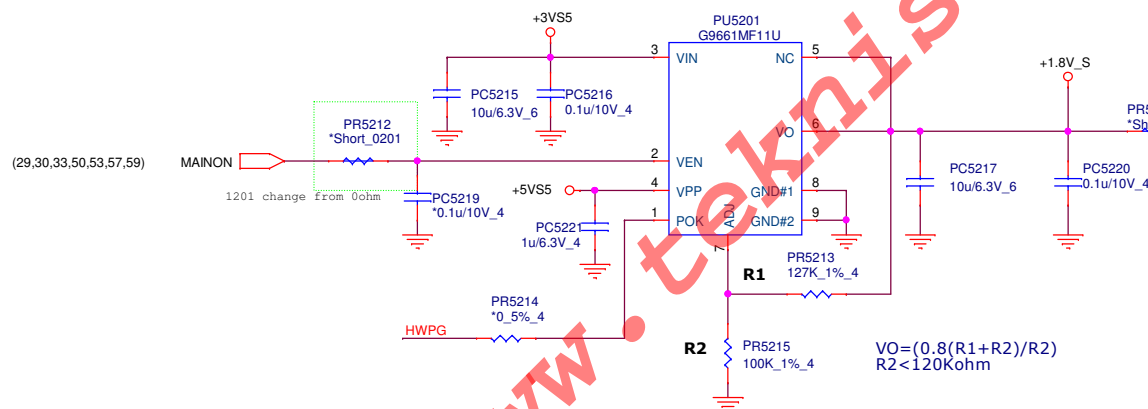
Imax: 0.24A



+1.8V +/- 5%

TDC: 1A

EDP: 2A



$$VO = (0.8(R1+R2))/R2$$

$$R2 < 120Kohm$$

+VIN	(28,37,40,51,52,53,54,55,56,57,60,63)
+3VS5	(10,12,14,16,29,30,33,35,36,37,40,41,43,44,50,52,53,57,59)
+5VS5	(10,28,33,37,38,40,44,52,53,54,55,56,57,59,60,61,62,63,64)
+1.0V_DEEP_SUS	(10,11,14,59)
+1.8V	(22,64)
+VCCSTPLL	(2,6,54)
+1.1V	(29,57)



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Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 5.5A

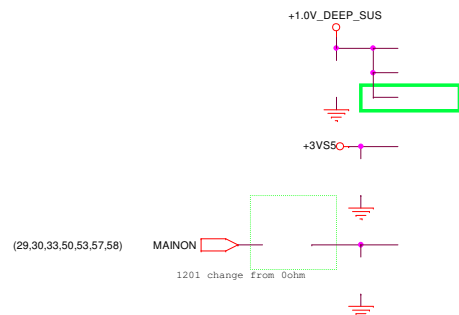
<= 10ms full load ready

Imax:5.5A

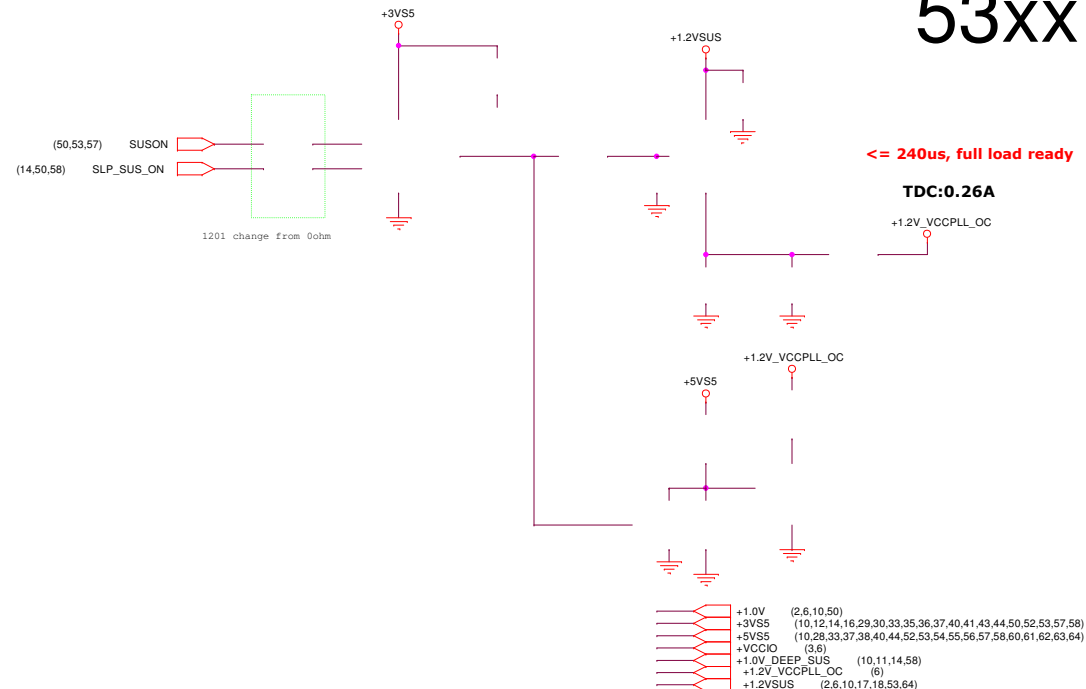
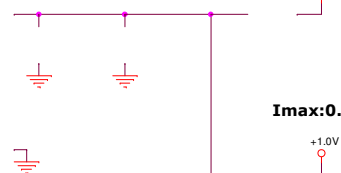
Imax:0.04A

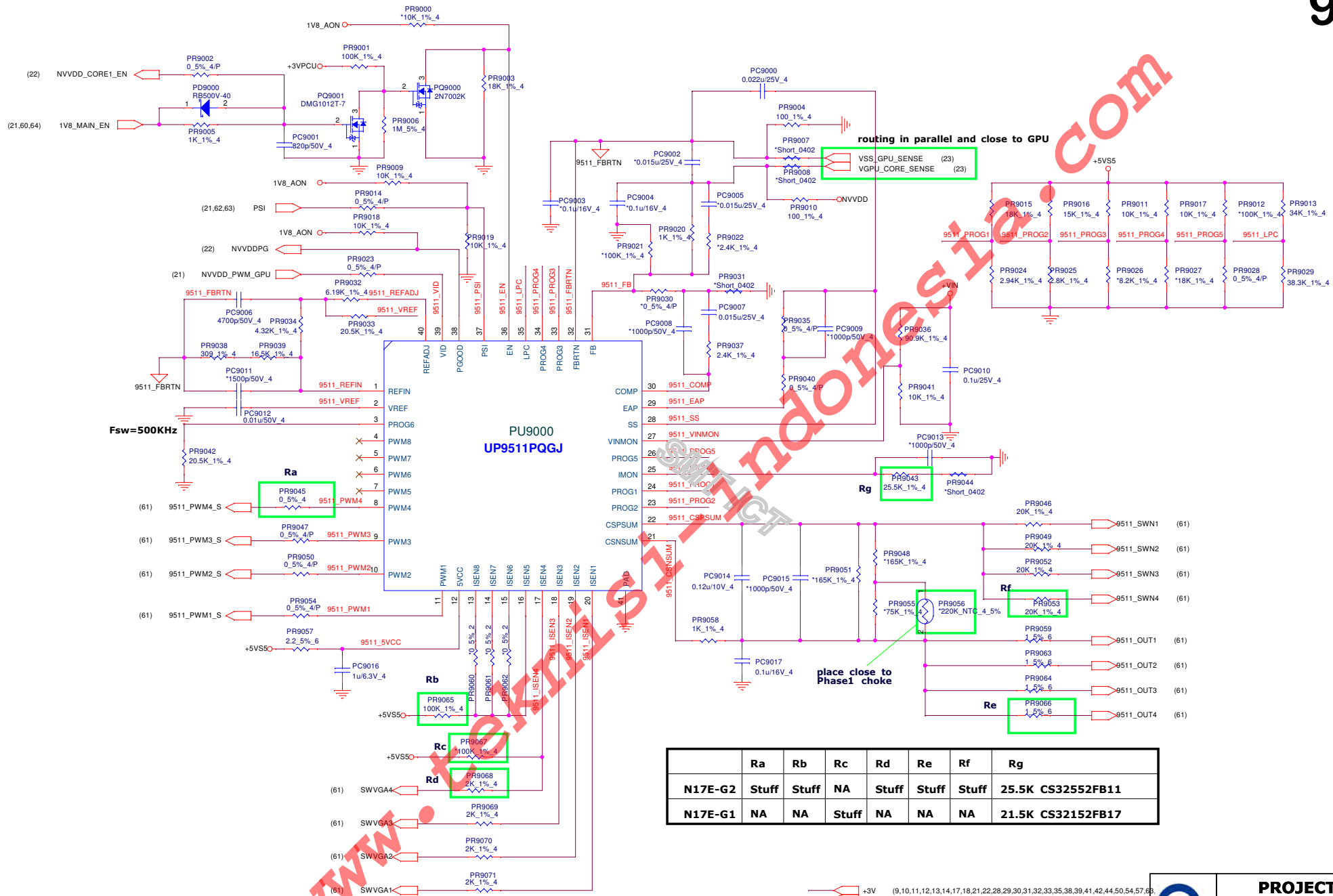
<= 240us, full load ready

TDC:0.26A



Reserve for separating +1.0V and VCCIO





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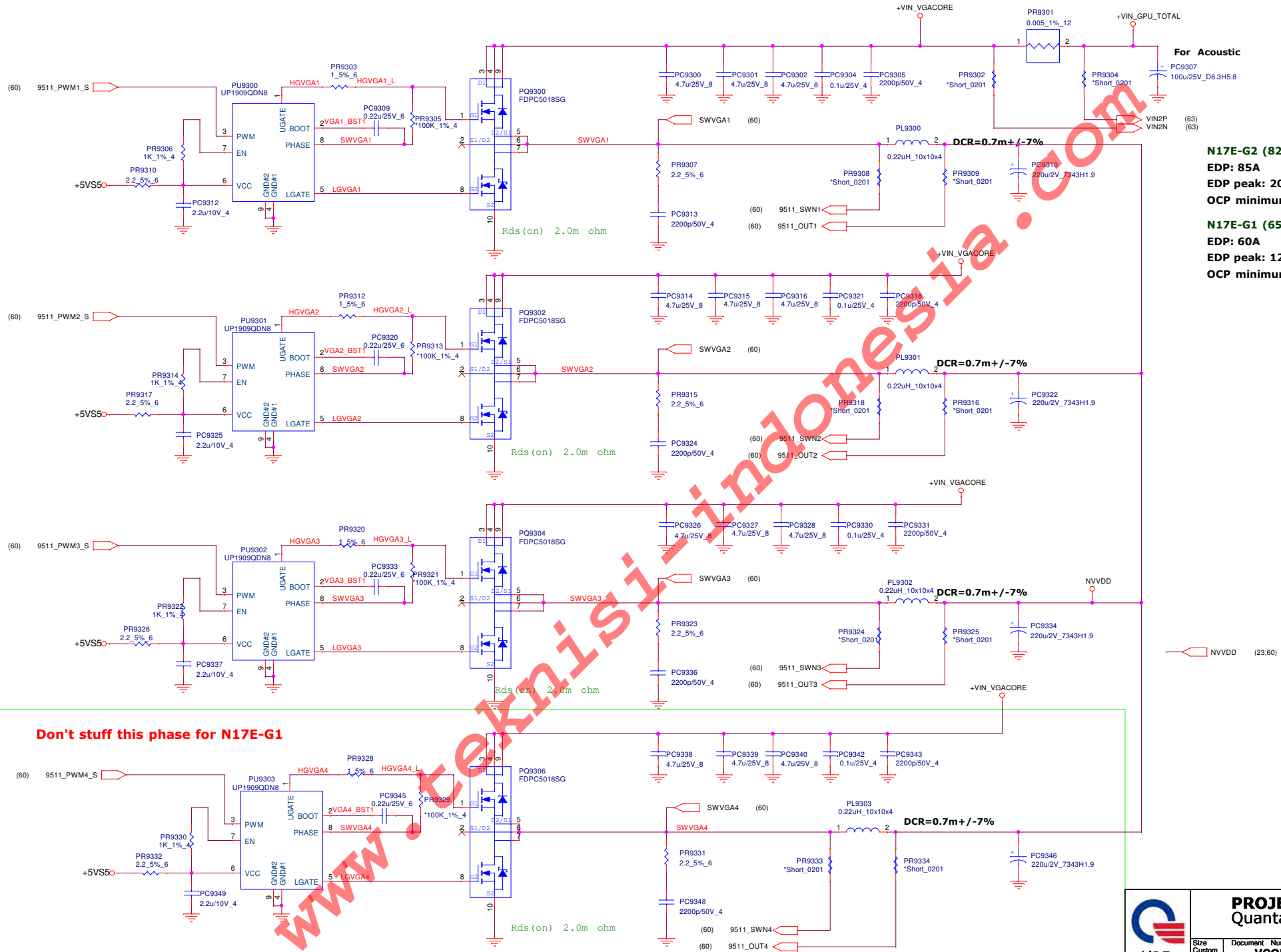
Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A
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For Acoustic

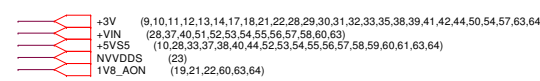
N17E-G2 (82W)
EDP: 85A
EDP peak: 203A
OCP minimum 245A

N17E-G1 (65W)
EDP: 60A
EDP peak: 127A
OCP minimum 197A



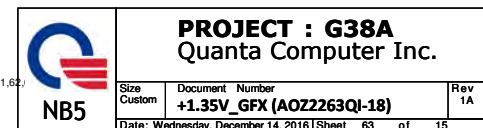
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Size	Document Number	Rev
Custom	+VCORE (NCP81151)	1A
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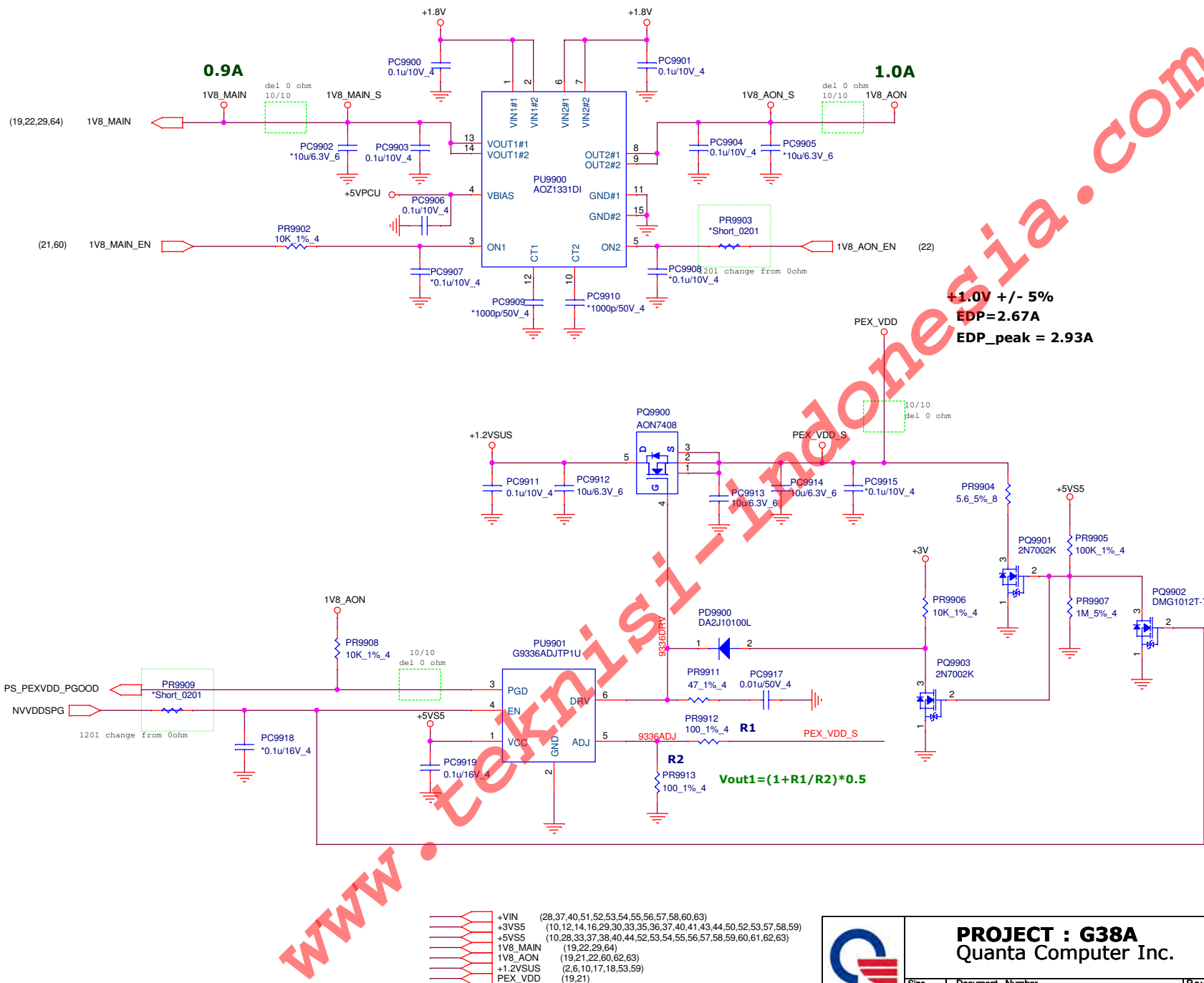


1.35V/1.55V +/- 5%
N17E-G2 (82W)
 EDP: 25A
 EDP: peak: 30.6A
 OCP minimum: 40A

N17E-G1 (65W)
 EDP: 19.8A
 EDP: peak: 32.2A
 OCP minimum: 42A



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